HSF Property:ROHS or Halogen-Free

GT		
R5279	SAMSUNG:6019B0971801	6013A0017501
R5279	HYNIX:6019B0971701	6013A0088503
GV2		
R5061	SAMSUNG:6019B1033601	6013A0107901
R5061	MICRON:6019B1033501	6013A0017501

	DIS SKU
MOUNT	R307 R4834
DEL	R309 R4832

	UMA SKU
MOUNT	R4819
DEL	R7496 R4636 R4638 R4639

U800 CN6050 IS NOT P/N

15SBGV2

SHARK BAY PGA

PV BUILD

2012.12.25

USB BOARD (6L)	1310A2548501	6050A2548501
USB BOARD (8L)	1310A2548601	6050A2548601
POWER BOARD (6L)	1310A2548701	6050A2548701
POWER BOARD (8L)	1310A2548801	6050A2548801
EMI BOARD (6L)	1310A2552101 1310A2552102	6050A2552101
EMI BOARD (8L)	1310A2552201 1310A2552202	6050A2552201

Platform	CPU	GPU	VRAM	PCB count	IEC P/N
UMA	37W (Quad) 47W (Quad)	NA	NA	6050A2547701(6L)	1310A2547701 1310A2547702
DIS	37W (Quad)	N14P-GV2 23*23 (25W)	128Mx16 DDR3 8pcs (2G) Samsung K4W2G1646E-BC1A (E-die) HP P/N: 601498-955 IEC P/N: 6019B1033601 Micron MT41J128M16JT-093G:K HP P/N: 601498-654 IEC P/N: 6019B1033601	6050A2548101 (8L)	1310A2548101 1310A2548102
DIS	47W (Quad)	N14P-GV2 23*23 (25W)	128Mx16 DDR3 8pcs (2G) Samsung K4W2G1646E-BC1A (E-die) HP P/N: 601498-955 IEC P/N: 6019B1033601 Micron MT41J128M16JT-093G:K HP P/N: 601498-654 IEC P/N: 6019B1033601		1310A2548105 1310A2548106

CHANGE NO.	REV
MV	A03
MV	A02
PV	A01
SI2	AX2
SI	AX1
DB2	X02
DB	X01

21-OCT-2002
2012.5.22
DATE

	EE	DATE	POWER	DATE
DRAWER				
DESIGN				
CHECK				
RESPONSIBLE				

SIZE= VER:
FILE NAME:
P/N XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Main Board

SIZE	CODE	DOCNUMBER	REV
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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
INDEX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	A01

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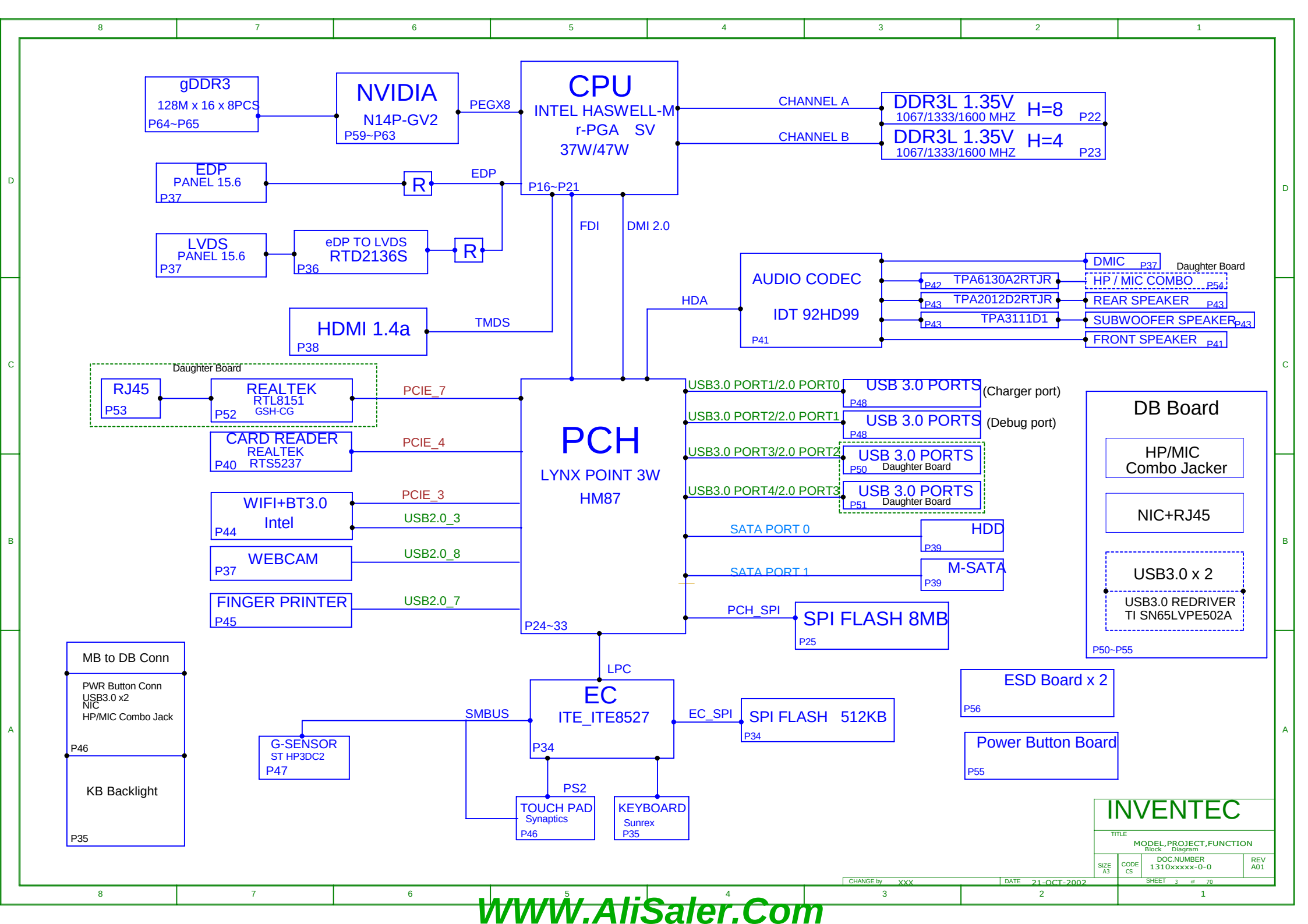

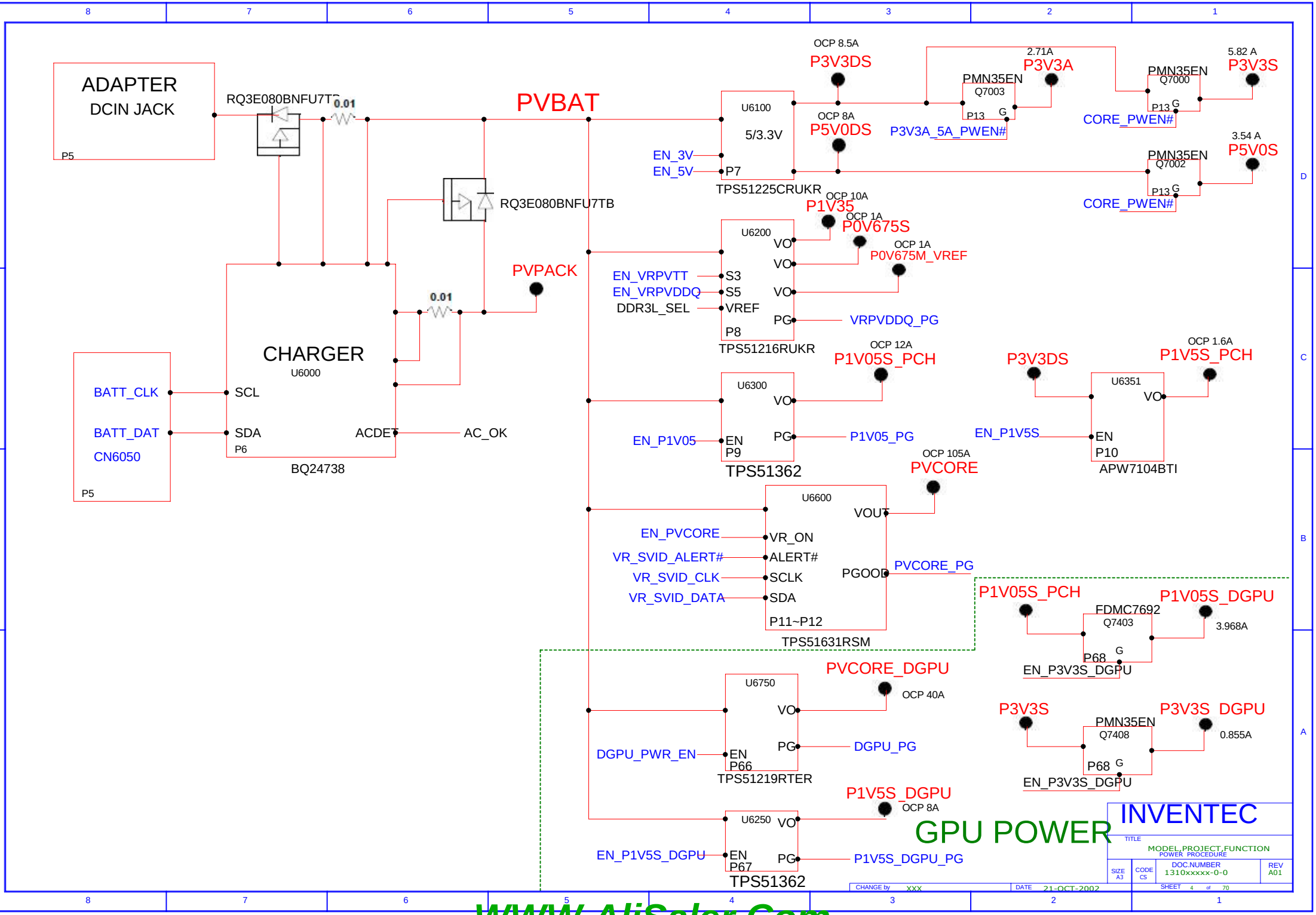

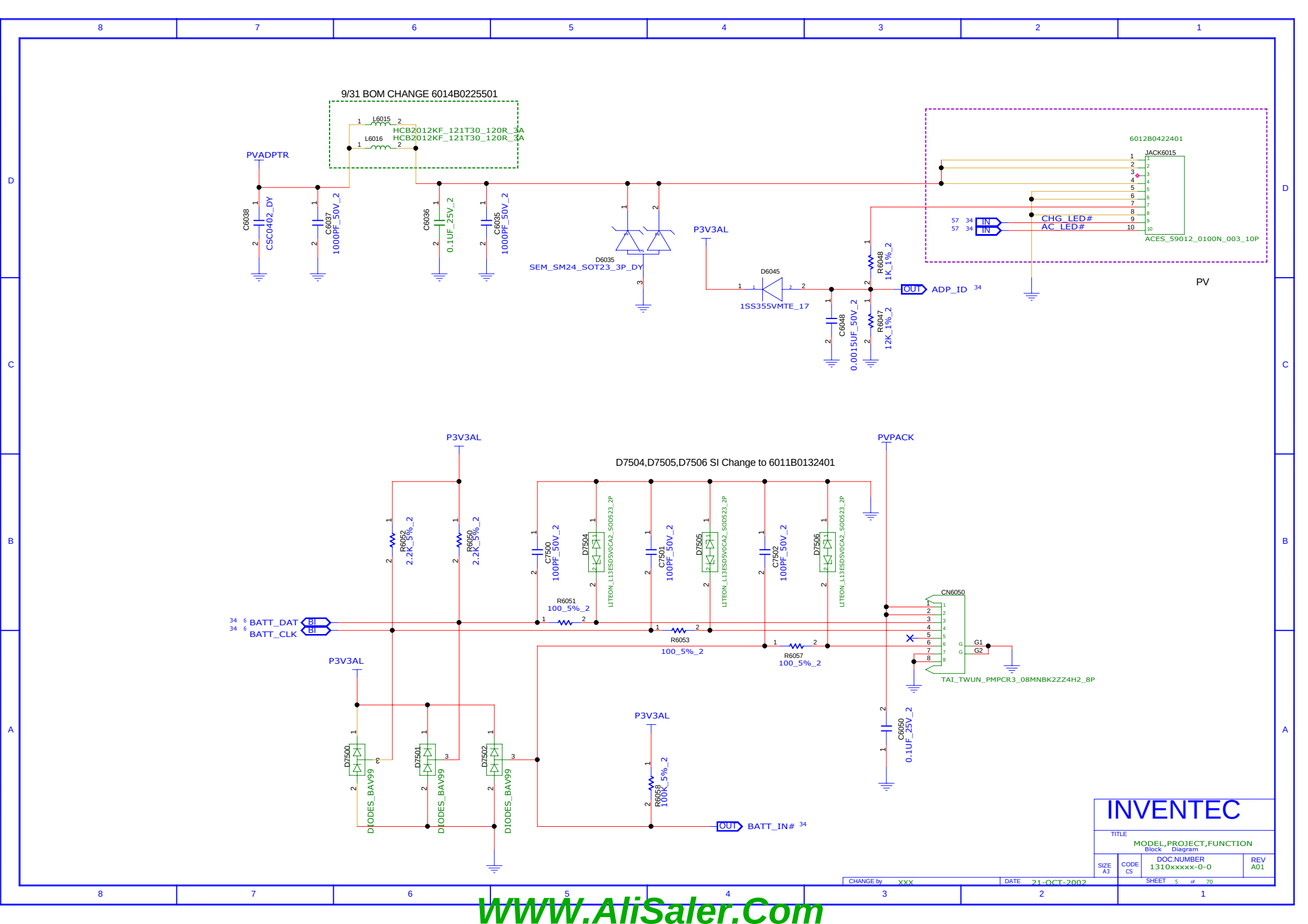

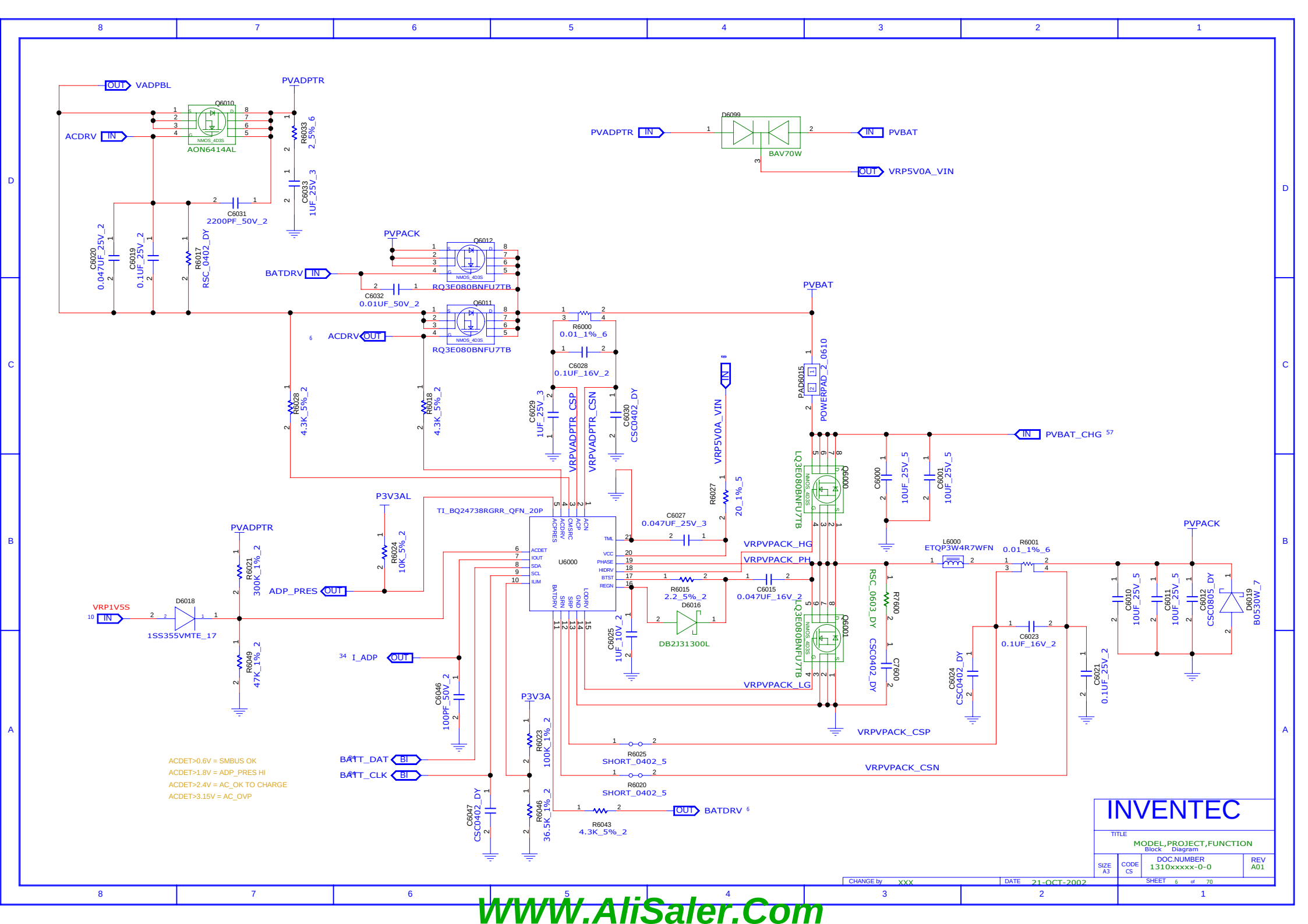

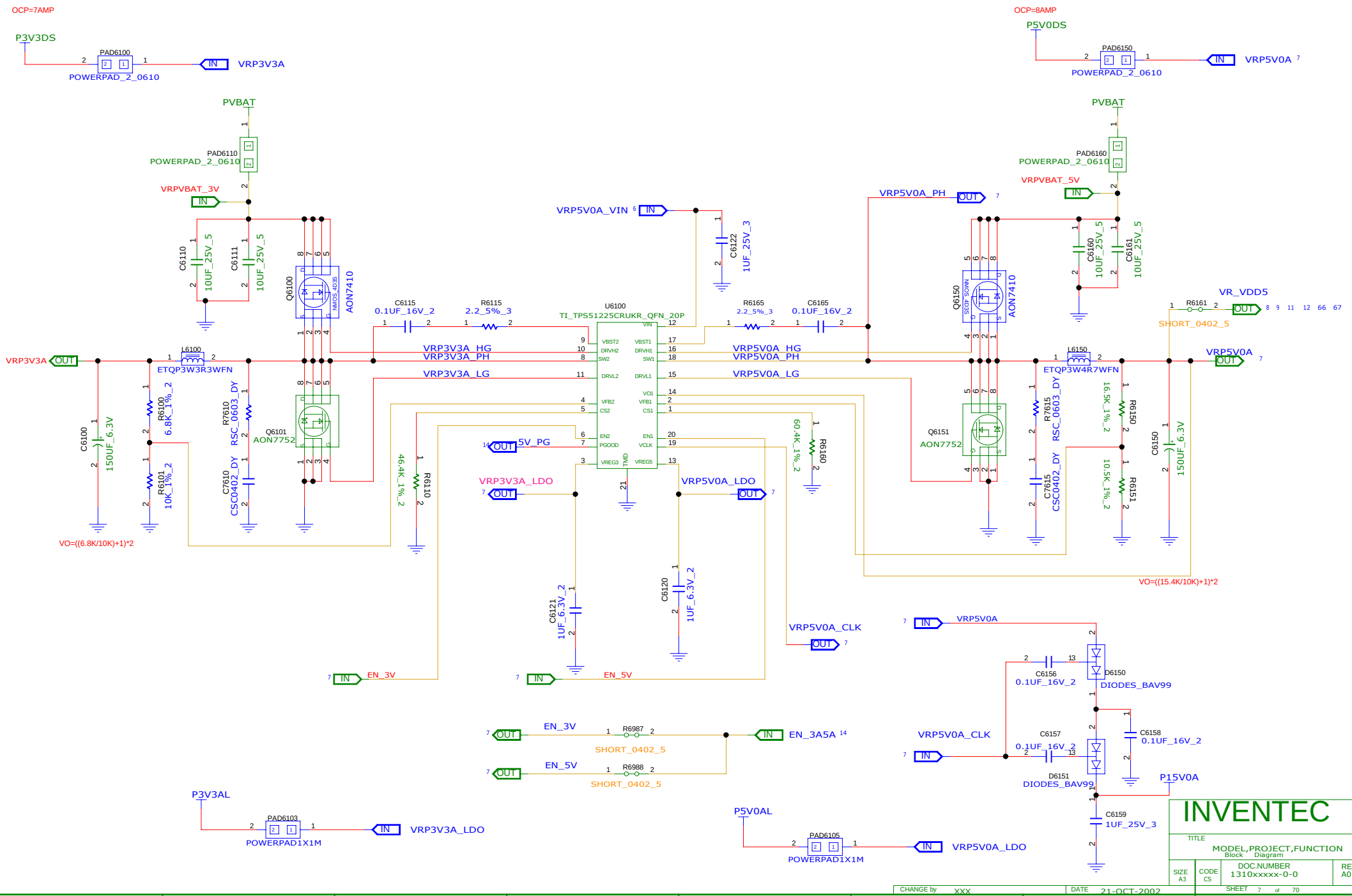

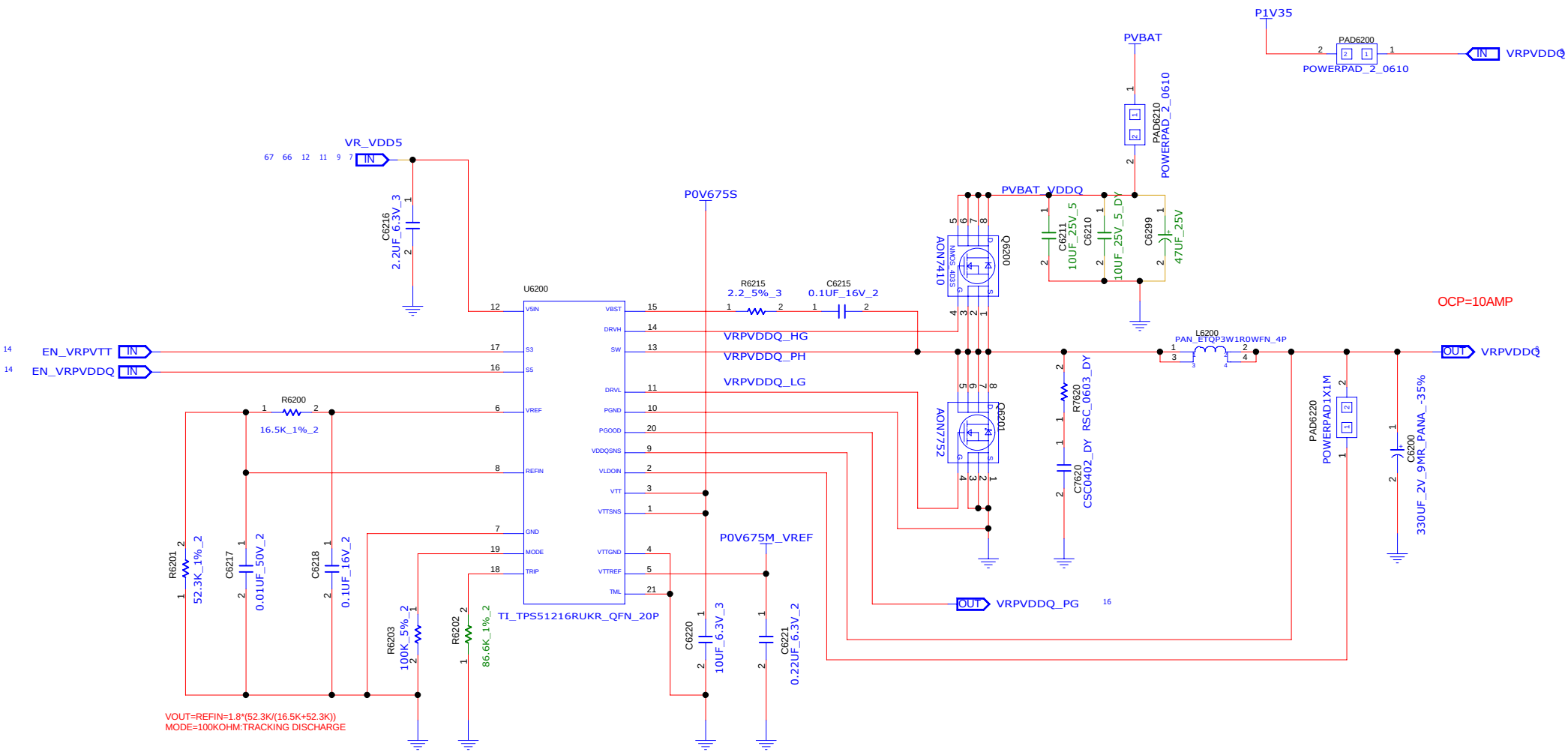

Table 1. S3/S5 Power State Control

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	A01

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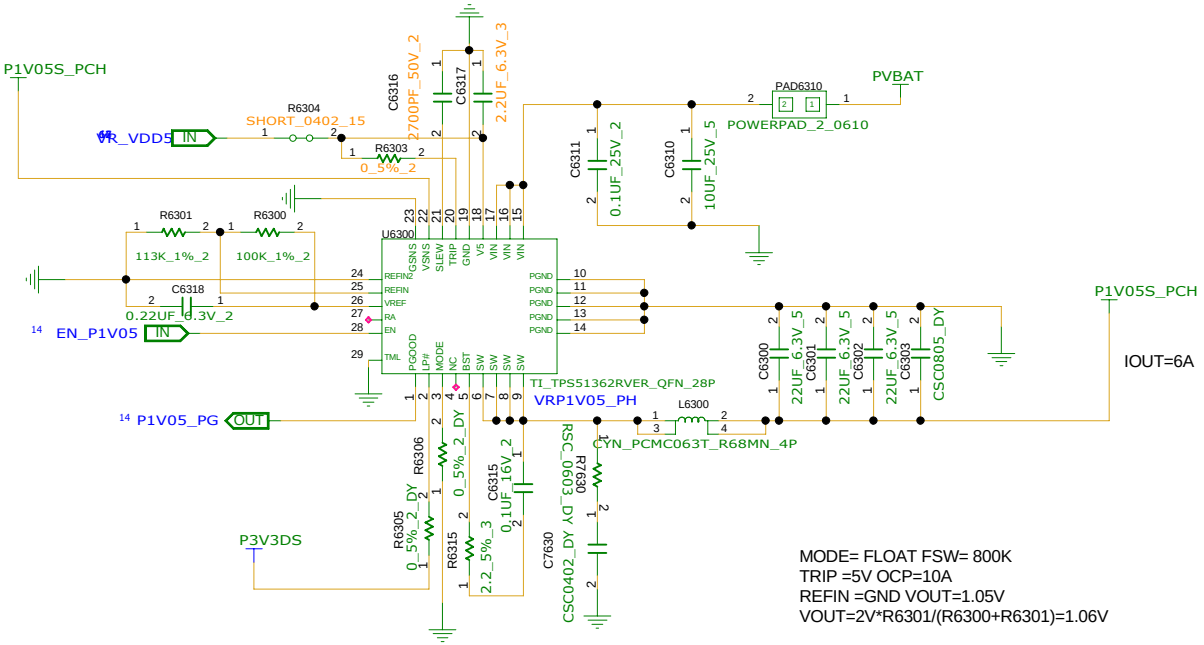

P1V05S-PCH	DEFAULT	INCREASE1%
R6301	0	113K_1%
R6300	DY	100K_1%

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	A01

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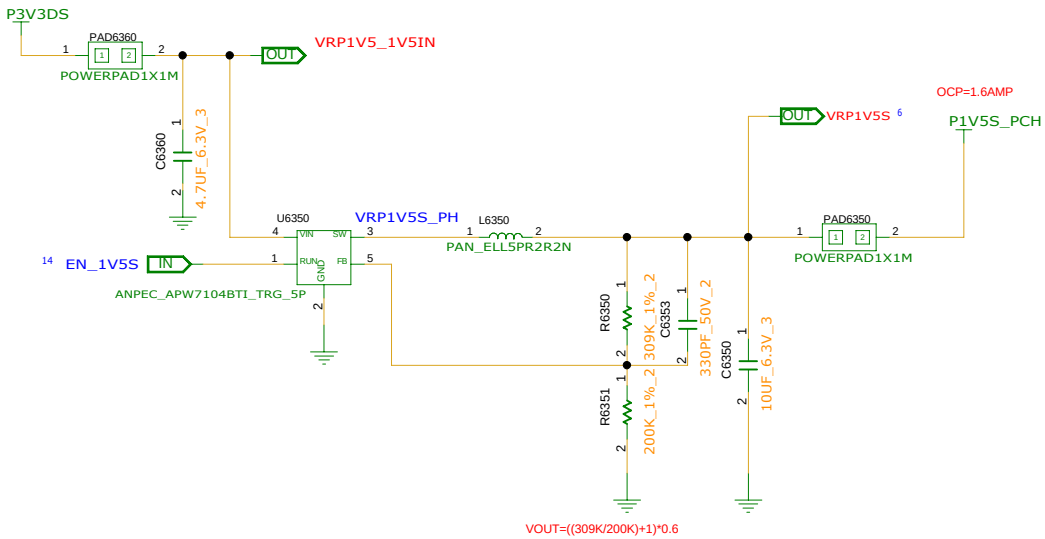

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	A01

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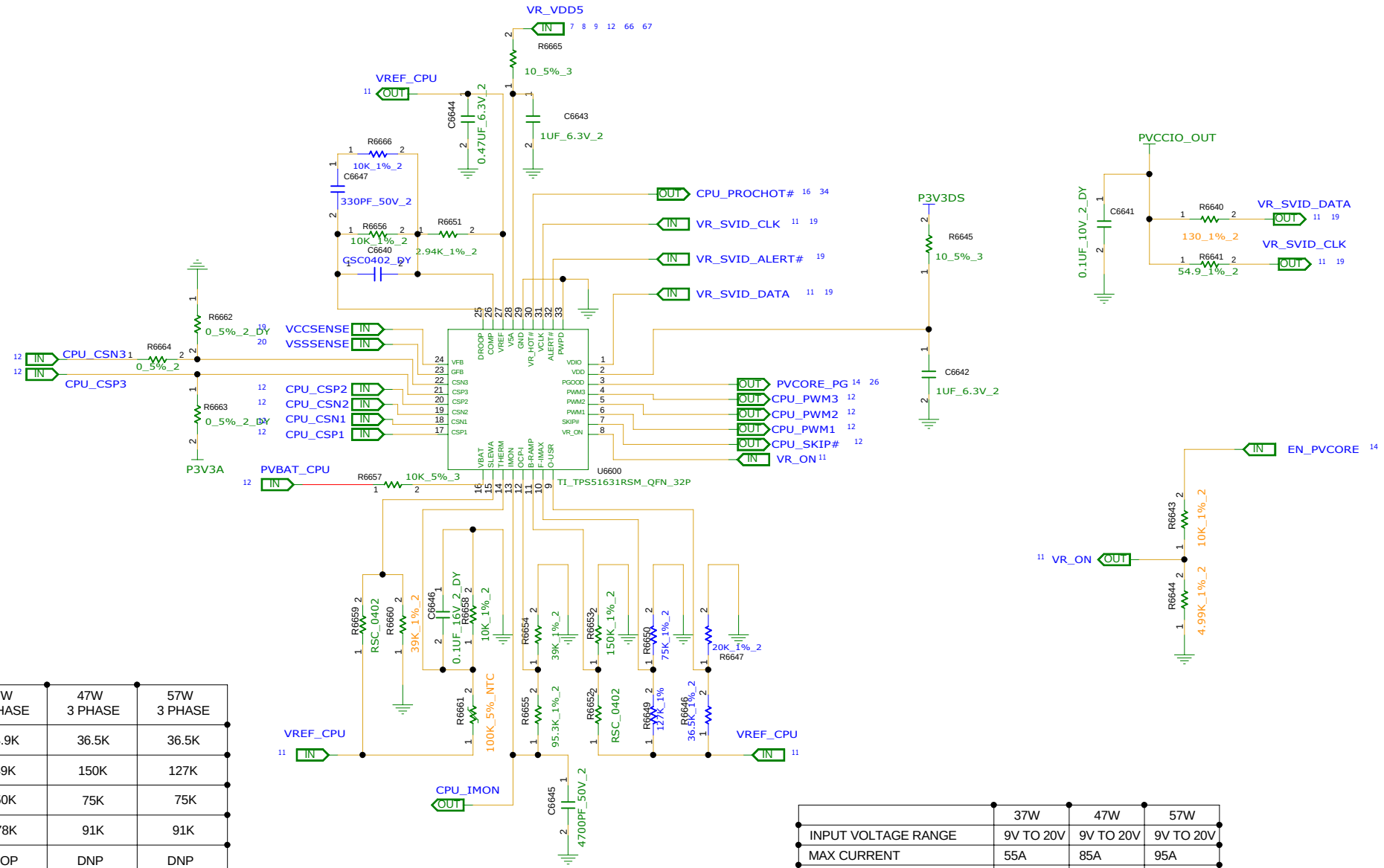

	37W 2 PHASE	47W 3 PHASE	57W 3 PHASE
R6646	64.9K	36.5K	36.5K
R6649	549K	150K	127K
R6650	150K	75K	75K
R6655	178K	91K	91K
R6662	POP	DNP	DNP
R6663	POP	DNP	DNP
R6664	DNP	POP	POP

	37W	47W	57W
INPUT VOLTAGE RANGE	9V TO 20V	9V TO 20V	9V TO 20V
MAX CURRENT	55A	85A	95A
THERMAL DESIGN CURRENT	21A	27A	33A
DYNAMIC CURRENT	35A	60A	60A
OVER CURRENT LEVEL	70A	105A	105A
SWITCHING FREQUENCY	1MHZ	800KHZ	800KHZ
BOOT VOLTAGE	1.7V	1.7V	1.7V
DC LOAD-LINE	1.5MOHM	1.5MOHM	1.5MOHM

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	A01

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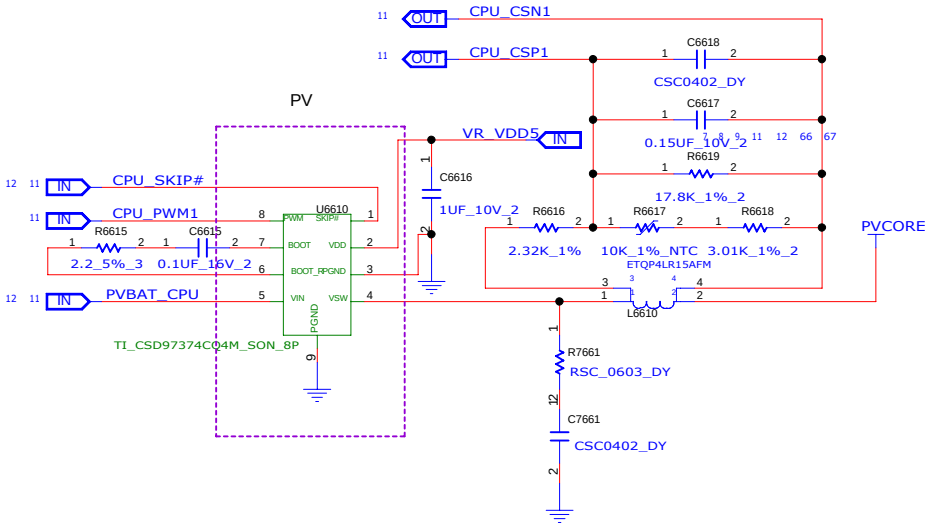

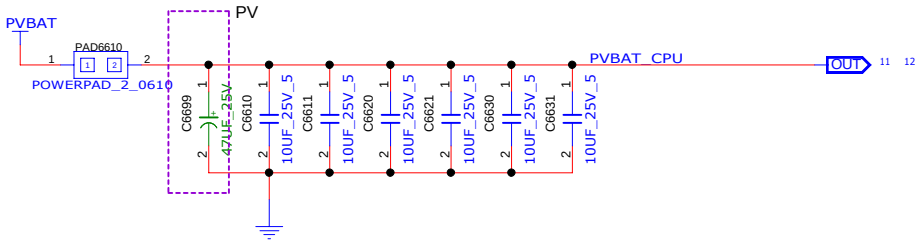

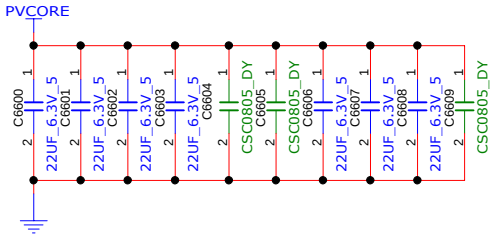

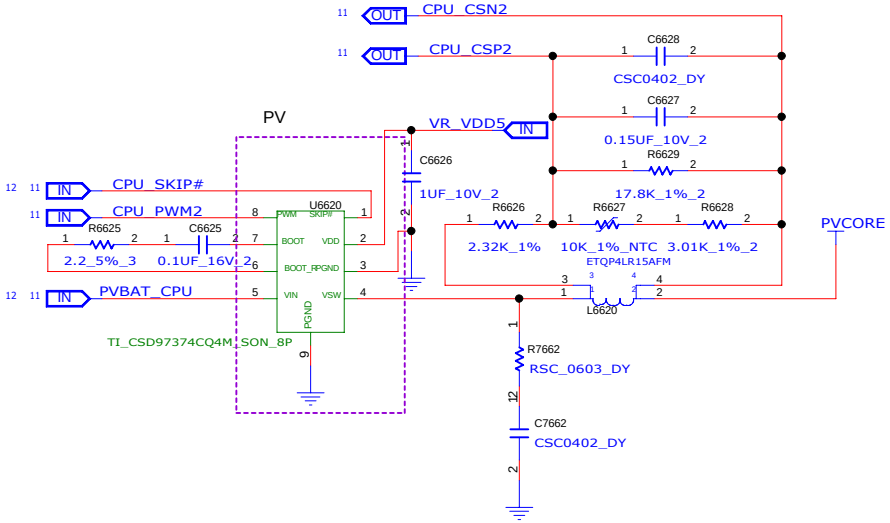

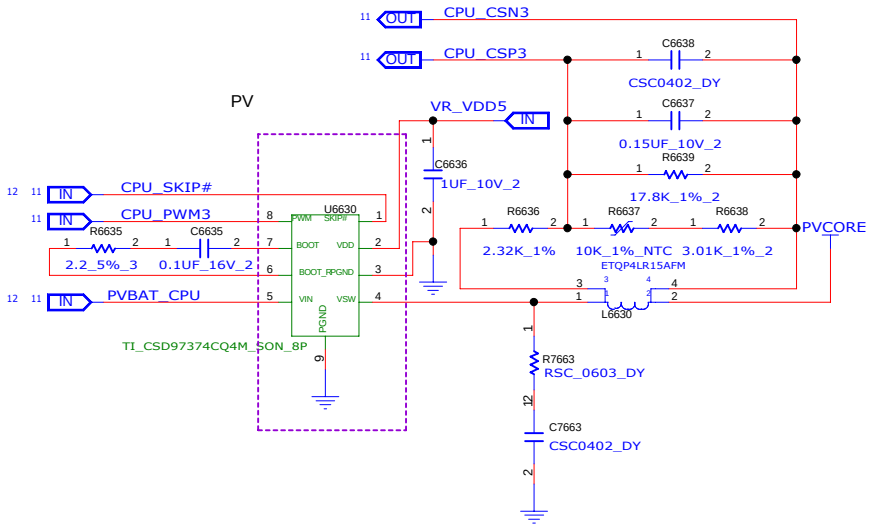

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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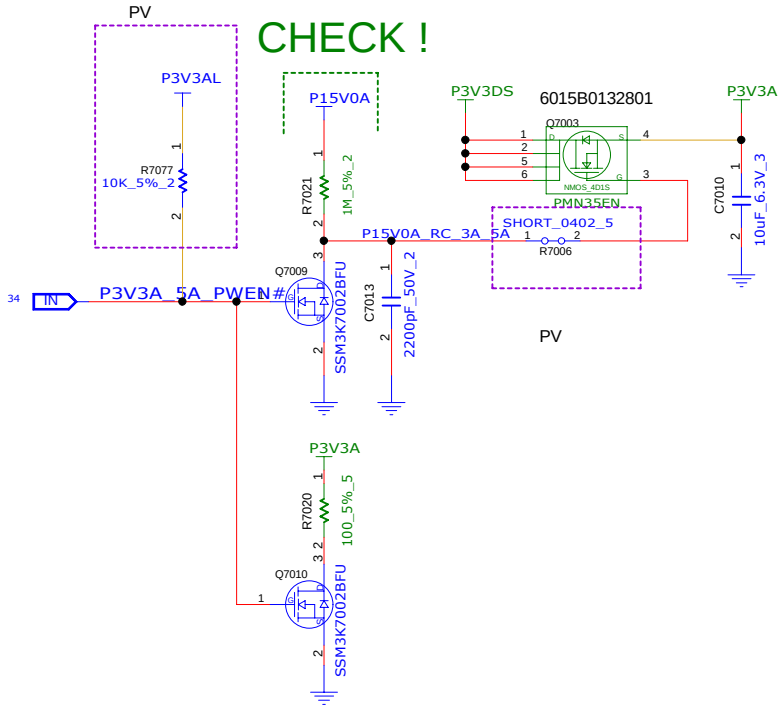
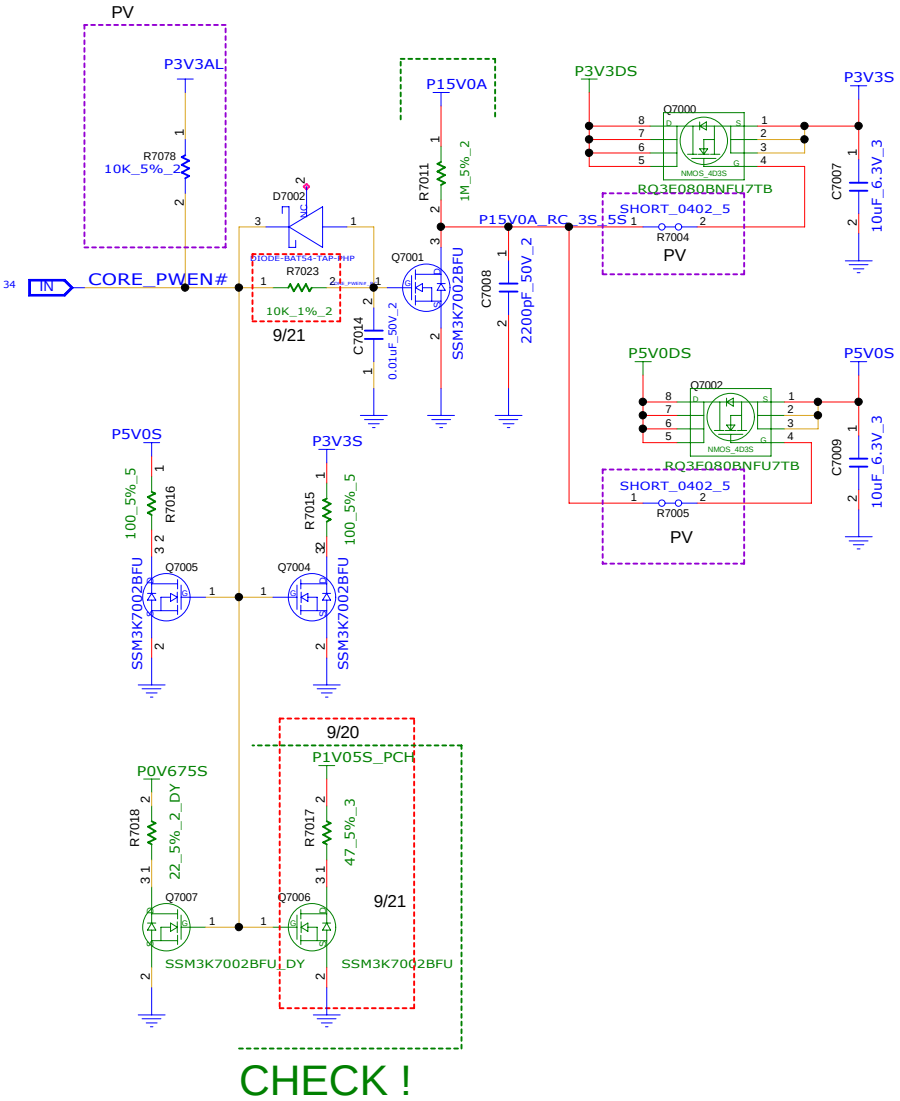
CHECK !

CHECK !





CHECK !

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	A01

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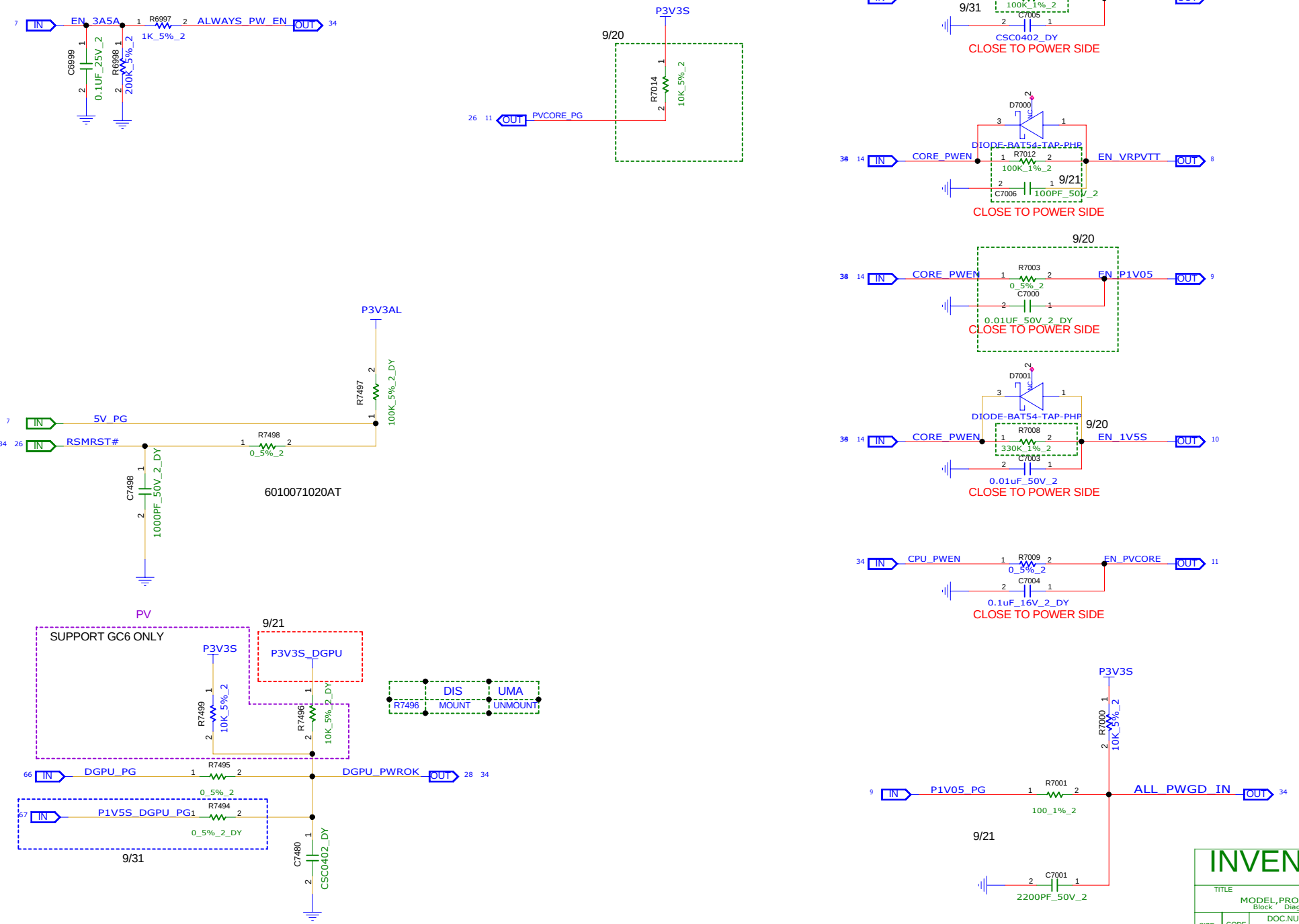

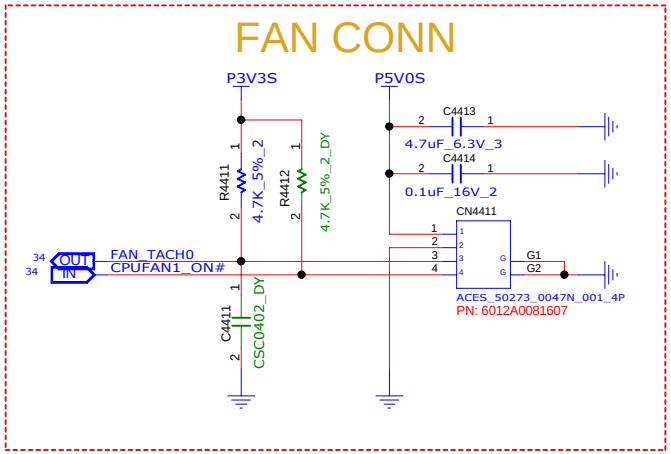

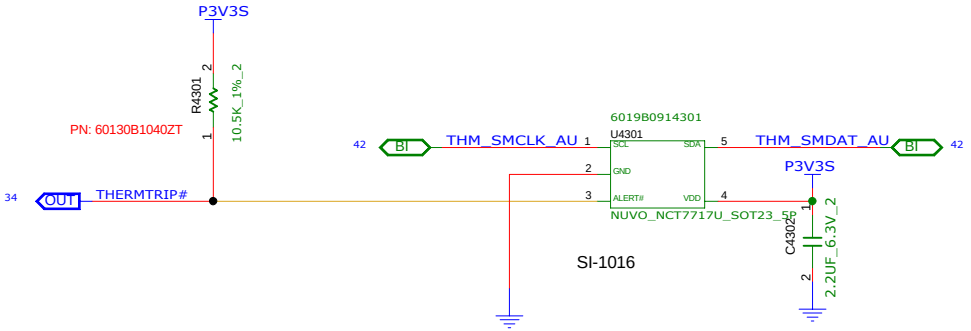

NCT7717U I2C/SMBUS ADDRESS IS 1001000XB (X IS R/W BIT)

PULL-UP RESISTOR		TEMPERATURE (℃)
ALERT	2KΩ	75
	7.5KΩ	90
	10.5KΩ	100
	14KΩ	105
	18.7KΩ	110

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
THERMAL & FAN

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	A01

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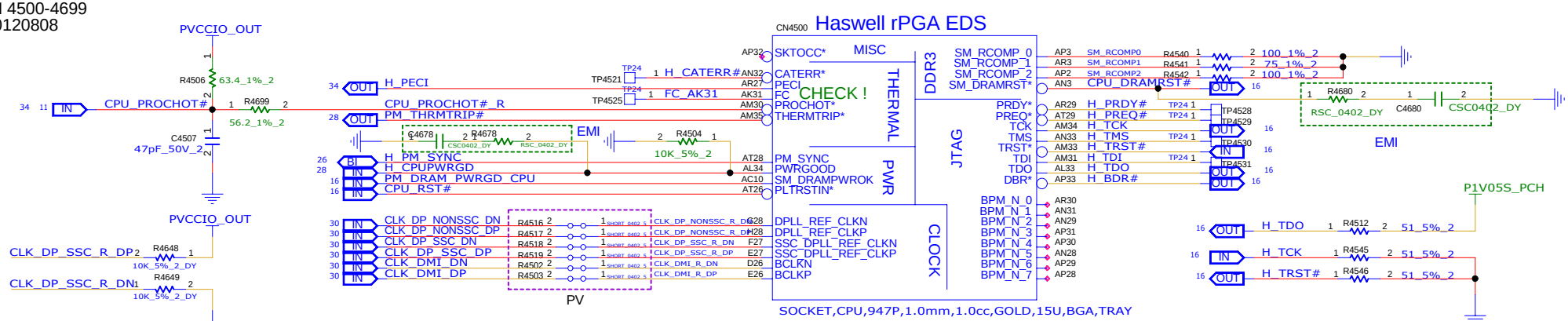
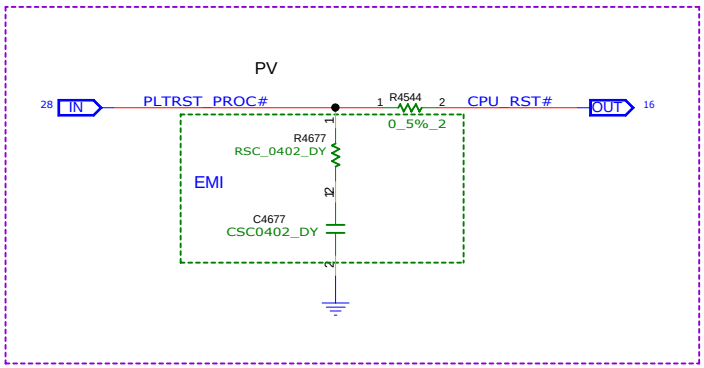
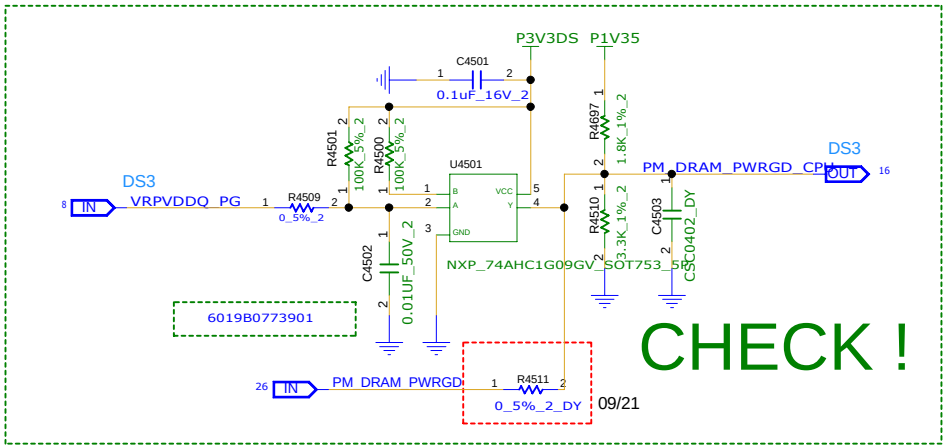
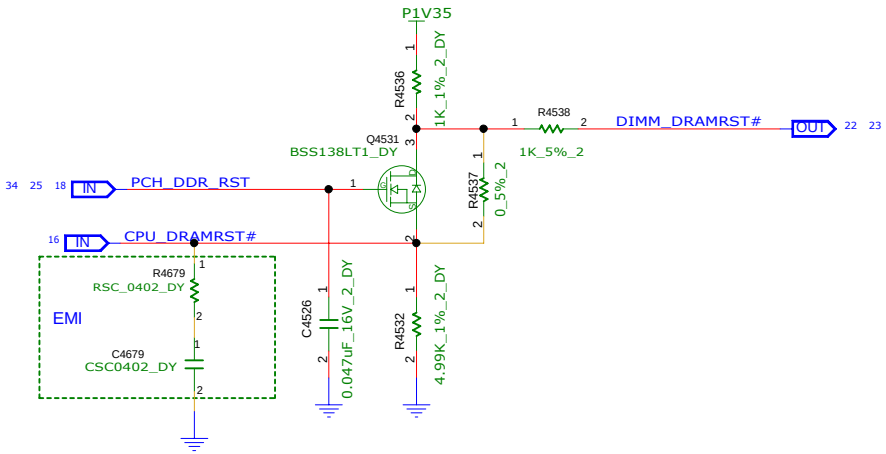
CPU
LOCATION 4500-4699
VER.01_20120808



CN4500
6026B0231701







INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV A01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 16 of 70	

CPU
LOCATION 4500-4699
VER.01_20120808

GV2

UMA DELETE

CN4500 Haswell rPGA EDS

PVCCIOA_OUT

R4645 24.9_1%_2

DMI_TX0_DN D21 DMI_RXN_0
DMI_TX1_DN C21 DMI_RXN_1
DMI_TX2_DN B21 DMI_RXN_2
DMI_TX3_DN A21 DMI_RXN_3

DMI_TX0_DP D20 DMI_RXP_0
DMI_TX1_DP C20 DMI_RXP_1
DMI_TX2_DP B20 DMI_RXP_2
DMI_TX3_DP A20 DMI_RXP_3

DMI_RX0_DN D18 DMI_TXN_0
DMI_RX1_DN C17 DMI_TXN_1
DMI_RX2_DN B17 DMI_TXN_2
DMI_RX3_DN A17 DMI_TXN_3

DMI_RX0_DP D17 DMI_TXP_0
DMI_RX1_DP C18 DMI_TXP_1
DMI_RX2_DP B18 DMI_TXP_2
DMI_RX3_DP A18 DMI_TXP_3

DMI

FDI_CSYNC H29 FDI_CSYNC
FDI_INT J29 FDI_INT

FDI

PEG

PEG_RCOMP E23 PEG_RCOMP
PEG_RXN_0 M29 PEG_RX0_C_DN
PEG_RXN_1 K28 PEG_RX1_C_DN
PEG_RXN_2 M31 PEG_RX2_C_DN
PEG_RXN_3 L30 PEG_RX3_C_DN
PEG_RXN_4 M33 PEG_RX4_C_DN
PEG_RXN_5 L32 PEG_RX5_C_DN
PEG_RXN_6 M35 PEG_RX6_C_DN
PEG_RXN_7 L34 PEG_RX7_C_DN
PEG_RXN_8 E29
PEG_RXN_9 D28
PEG_RXN_10 E31
PEG_RXN_11 D30
PEG_RXN_12 E35
PEG_RXN_13 D34
PEG_RXN_14 E33
PEG_RXN_15 E32

PEG_RXP_0 L29 PEG_RX0_C_DP
PEG_RXP_1 L28 PEG_RX1_C_DP
PEG_RXP_2 L31 PEG_RX2_C_DP
PEG_RXP_3 K30 PEG_RX3_C_DP
PEG_RXP_4 L33 PEG_RX4_C_DP
PEG_RXP_5 K32 PEG_RX5_C_DP
PEG_RXP_6 L35 PEG_RX6_C_DP
PEG_RXP_7 K34 PEG_RX7_C_DP
PEG_RXP_8 F29
PEG_RXP_9 E28
PEG_RXP_10 F31
PEG_RXP_11 E30
PEG_RXP_12 F35
PEG_RXP_13 E34
PEG_RXP_14 F33
PEG_RXP_15 D32

PEG_TXN_0 H35 PEG_TX0_DN
PEG_TXN_1 H34 PEG_TX1_DN
PEG_TXN_2 J33 PEG_TX2_DN
PEG_TXN_3 H32 PEG_TX3_DN
PEG_TXN_4 J31 PEG_TX4_DN
PEG_TXN_5 G30 PEG_TX5_DN
PEG_TXN_6 C33 PEG_TX6_DN
PEG_TXN_7 B32 PEG_TX7_DN
PEG_TXN_8 B31
PEG_TXN_9 A30
PEG_TXN_10 B29
PEG_TXN_11 A28
PEG_TXN_12 B27
PEG_TXN_13 A26
PEG_TXN_14 B25
PEG_TXN_15 A24

PEG_TXP_0 J35 PEG_TX0_DP
PEG_TXP_1 G34 PEG_TX1_DP
PEG_TXP_2 H33 PEG_TX2_DP
PEG_TXP_3 G32 PEG_TX3_DP
PEG_TXP_4 H31 PEG_TX4_DP
PEG_TXP_5 H30 PEG_TX5_DP
PEG_TXP_6 B33 PEG_TX6_DP
PEG_TXP_7 A32 PEG_TX7_DP
PEG_TXP_8 C31
PEG_TXP_9 B30
PEG_TXP_10 C29
PEG_TXP_11 B28
PEG_TXP_12 C27
PEG_TXP_13 B26
PEG_TXP_14 C25
PEG_TXP_15 B24

LOTES_AZIF0012_P001B_947P

CLOSE TO CPU

PEG_TX7_DN C4688 0.22UF_16V_2 PEG_TX7_C_DN
PEG_TX6_DN C4689 0.22UF_16V_2 PEG_TX6_C_DN
PEG_TX5_DN C4690 0.22UF_16V_2 PEG_TX5_C_DN
PEG_TX4_DN C4691 0.22UF_16V_2 PEG_TX4_C_DN
PEG_TX3_DN C4693 0.22UF_16V_2 PEG_TX3_C_DN
PEG_TX2_DN C4694 0.22UF_16V_2 PEG_TX2_C_DN
PEG_TX1_DN C4695 0.22UF_16V_2 PEG_TX1_C_DN
PEG_TX0_DN C4692 0.22UF_16V_2 PEG_TX0_C_DN

PEG_TX7_DP C4696 0.22UF_16V_2 PEG_TX7_C_DP
PEG_TX6_DP C4697 0.22UF_16V_2 PEG_TX6_C_DP
PEG_TX5_DP C4698 0.22UF_16V_2 PEG_TX5_C_DP
PEG_TX4_DP C4699 0.22UF_16V_2 PEG_TX4_C_DP
PEG_TX3_DP C4504 0.22UF_16V_2 PEG_TX3_C_DP
PEG_TX2_DP C4505 0.22UF_16V_2 PEG_TX2_C_DP
PEG_TX1_DP C4506 0.22UF_16V_2 PEG_TX1_C_DP
PEG_TX0_DP C4508 0.22UF_16V_2 PEG_TX0_C_DP

FOR DGPU SCREW

S5000 SCREW330_600_1P
S5001 SCREW330_600_1P
S5002 SCREW330_600_1P
S5003 SCREW330_600_1P

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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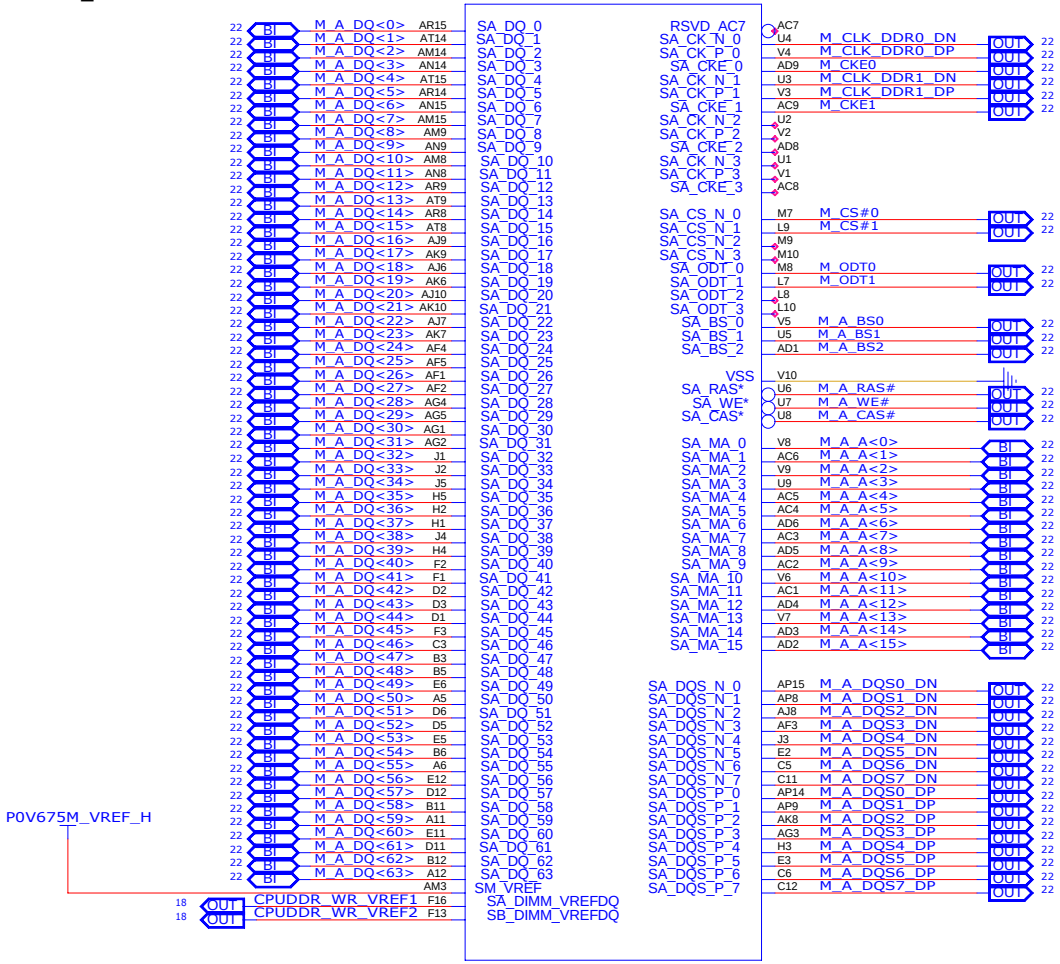
CPU
LOCATION 4500-4699
VER.01_20120808

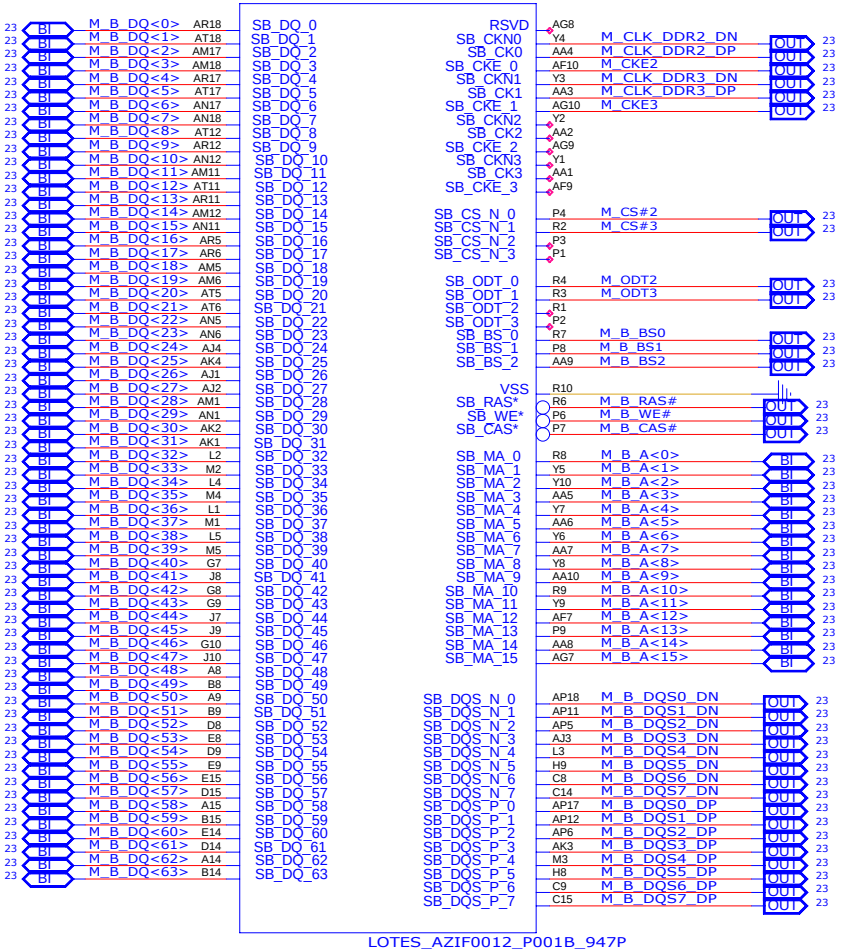
Haswell rPGA EDS

CN4500



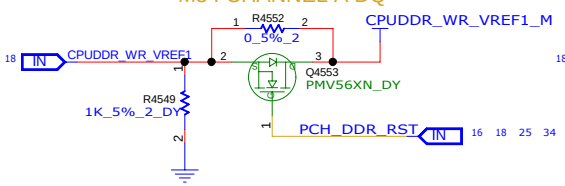
Haswell rPGA EDS

CN4500

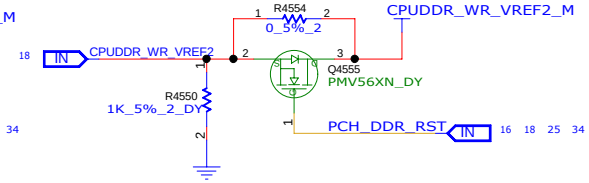


CN4500
6026B0231701

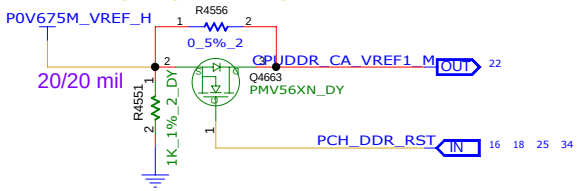
M3 : CHANNEL A DQ



M3 : CHANNEL B DQ



M3 : 2 CHANNEL CA



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	A01

CHANGE by XXX | DATE 21-OCT-2002 | SHEET 18 of 70

CPU
LOCATION 4500-4699
VER.01_20120808

CHECK! intel seems to disable CPU S3 power reduction.

NA

6010B0106701

6010B0140601

CN4500 Haswell rPGA EDS

LOTES_AZIF0012_P001B_947P

OPEN

close to CPU

PV

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3 | CODE CS | DOC.NUMBER 1310xxxxx-0-0 | REV A01

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CPU
LOCATION 4500-4699
VER.01_20120808

CN4500

Haswell rPGA EDS

A10	VSS	VSS	AK34
A13	VSS	VSS	AK5
A16	VSS	VSS	AL1
A19	VSS	VSS	AL10
A22	VSS	VSS	AL11
A25	VSS	VSS	AL12
A27	VSS	VSS	AL14
A29	VSS	VSS	AL15
A3	VSS	VSS	AL17
A31	VSS	VSS	AL18
A33	VSS	VSS	AL2
A4	VSS	VSS	AL20
A7	VSS	VSS	AL21
AA11	VSS	VSS	AL23
AA25	VSS	VSS	E22
AA27	VSS	VSS	AL3
AA31	VSS	VSS	AL4
AA29	VSS	VSS	AL5
AB1	VSS	VSS	AL6
AB10	VSS	VSS	AL7
AA33	VSS	VSS	AL8
AA35	VSS	VSS	AL9
AB3	VSS	VSS	AM10
AC25	VSS	VSS	AM13
AC27	VSS	VSS	AM16
AB4	VSS	VSS	AM19
AB6	VSS	VSS	E25
AB7	VSS	VSS	AM32
AB9	VSS	VSS	AM4
AC11	VSS	VSS	AM7
AD11	VSS	VSS	AN10
AC29	VSS	VSS	AN13
AC31	VSS	VSS	AN16
AC33	VSS	VSS	AN19
AC35	VSS	VSS	AN2
AD7	VSS	VSS	AN21
AE1	VSS	VSS	AN24
AE10	VSS	VSS	AN27
AE25	VSS	VSS	AN30
AE29	VSS	VSS	AN34
AE3	VSS	VSS	AN4
AE27	VSS	VSS	AN7
AE35	VSS	VSS	AP1
AE4	VSS	VSS	AP10
AE6	VSS	VSS	AP13
AE7	VSS	VSS	AP16
AE9	VSS	VSS	AP19
AF11	VSS	VSS	AP4
AF6	VSS	VSS	AP7
AF8	VSS	VSS	W25
AG11	VSS	VSS	AR10
AG25	VSS	VSS	AR13
AE31	VSS	VSS	AR16
AG31	VSS	VSS	AR19
AE33	VSS	VSS	AR2
AG6	VSS	VSS	AR22
AH1	VSS	VSS	AR25
AH10	VSS	VSS	AR28
AH2	VSS	VSS	AR31
AG27	VSS	VSS	AR34
AG29	VSS	VSS	AR4
AH3	VSS	VSS	AR7
AG33	VSS	VSS	AT10
AG35	VSS	VSS	AT13
AH4	VSS	VSS	AT16
AH5	VSS	VSS	AT19
AH6	VSS	VSS	AT21
AH7	VSS	VSS	AT24
AH8	VSS	VSS	AT27
AH9	VSS	VSS	AT3
AJ11	VSS	VSS	AT30
AJ5	VSS	VSS	AT4
AK11	VSS	VSS	AT7
AK25	VSS	VSS	B10
AK26	VSS	VSS	B13
AK28	VSS	VSS	B16
AK29	VSS	VSS	B19
AK30	VSS	VSS	B2
AK32	VSS	VSS	B22
E19	VSS		

LOTES_AZIF0012_P001B_947P

CN4500

Haswell rPGA EDS

B34	VSS	VSS	K10
B4	VSS	VSS	K2
B7	VSS	VSS	K29
C1	VSS	VSS	K3
C10	VSS	VSS	K31
C13	VSS	VSS	K33
C16	VSS	VSS	K35
C19	VSS	VSS	K4
C2	VSS	VSS	K5
C22	VSS	VSS	K7
C24	VSS	VSS	K8
C26	VSS	VSS	K9
C28	VSS	VSS	L11
C30	VSS	VSS	L26
C32	VSS	VSS	L6
C34	VSS	VSS	M11
C4	VSS	VSS	M26
C7	VSS	VSS	M28
D10	VSS	VSS	M30
D13	VSS	VSS	M32
D16	VSS	VSS	M34
D19	VSS	VSS	M6
D22	VSS	VSS	N1
D25	VSS	VSS	N10
D27	VSS	VSS	N2
D29	VSS	VSS	N29
D31	VSS	VSS	N3
D33	VSS	VSS	N31
D35	VSS	VSS	N33
D4	VSS	VSS	N35
D7	VSS	VSS	N4
E1	VSS	VSS	N5
E10	VSS	VSS	N6
E13	VSS	VSS	N7
E16	VSS	VSS	N9
E4	VSS	VSS	P11
E7	VSS	VSS	P26
F10	VSS	VSS	P5
F11	VSS	VSS	R11
F12	VSS	VSS	R26
F14	VSS	VSS	R28
F15	VSS	VSS	R30
F17	VSS	VSS	R32
F18	VSS	VSS	R34
F20	VSS	VSS	R5
F21	VSS	VSS	T1
F23	VSS	VSS	T10
F24	VSS	VSS	T29
F26	VSS	VSS	T3
F28	VSS	VSS	T31
F30	VSS	VSS	T33
F32	VSS	VSS	T35
F34	VSS	VSS	T4
F4	VSS	VSS	T6
F6	VSS	VSS	T7
F7	VSS	VSS	T9
F8	VSS	VSS	U11
F9	VSS	VSS	U27
G1	VSS	VSS	V11
G11	VSS	VSS	V28
G2	VSS	VSS	V30
G27	VSS	VSS	V32
G29	VSS	VSS	V34
G3	VSS	VSS	W1
G31	VSS	VSS	W10
G33	VSS	VSS	W3
G35	VSS	VSS	W35
G4	VSS	VSS	W4
G5	VSS	VSS	W6
H10	VSS	VSS	W7
H26	VSS	VSS	W9
H6	VSS	VSS	Y11
H7	VSS	VSS	H11
J11	VSS	VSS	AL24
J26	VSS	VSS	F19
J28	VSS	VSS	T26
J30	VSS	VSS_SENSE	AK35
J32	VSS	RSVD	AK33
J34	VSS		
J6	VSS		
K1	VSS		

LOTES_AZIF0012_P001B_947P

PV
close to CPU

R4632
SHORT_0402_5
VSSSENSE_R
VSSSENSE
OUT
11

R4633
100_1%_2

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	A01

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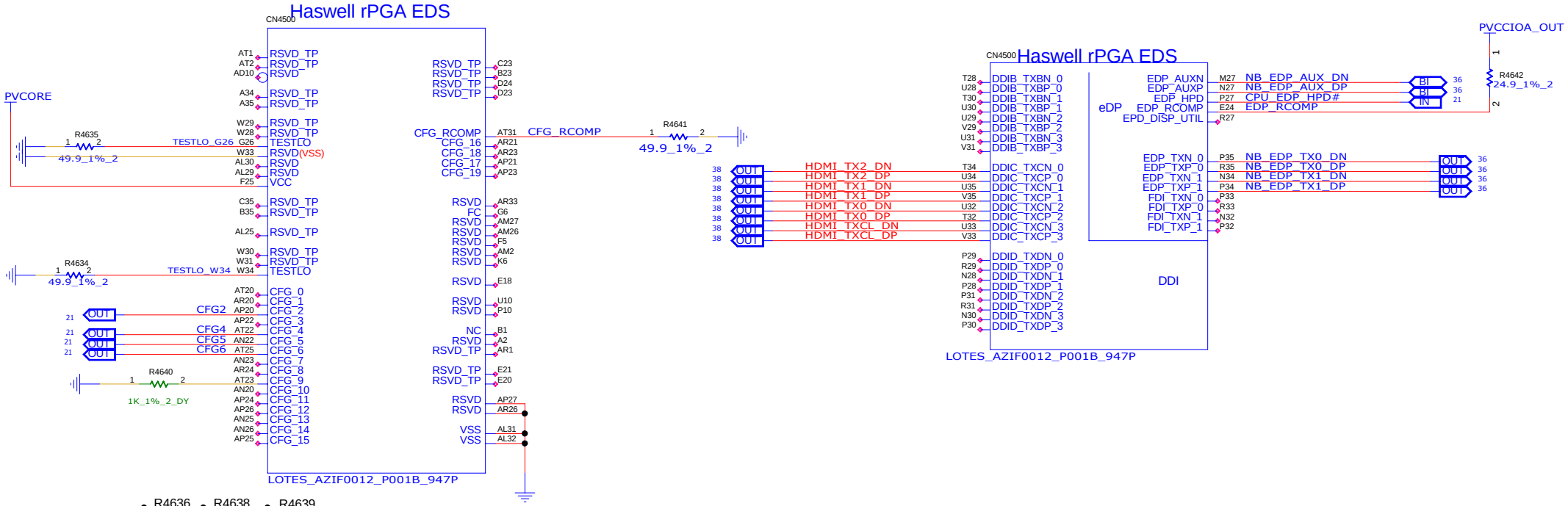
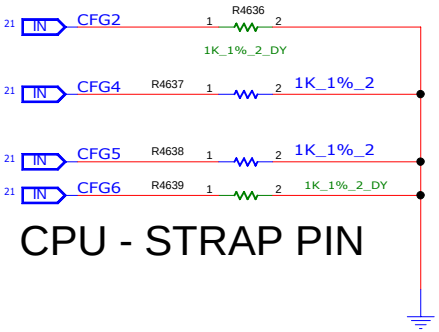
CPU
LOCATION 4500-4699
VER.01_20120808

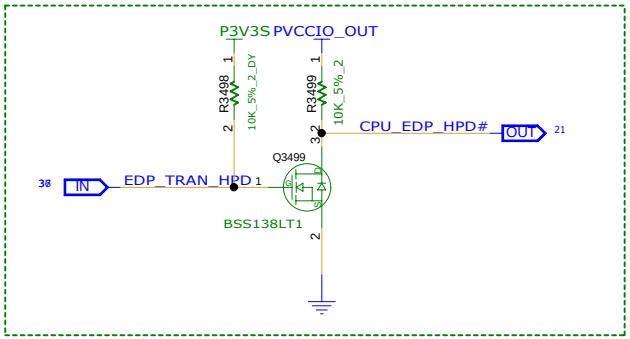


	R4636	R4638	R4639
GV2	OPEN	MOUNT	MOUNT
GT	MOUNT	OPEN	OPEN
UMA	OPEN	OPEN	OPEN



CPU - STRAP PIN

- **CFG[1:0]:** Reserved configuration lane. A test point may be placed on the board for these lanes.
- **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal.
  - 1 = Normal operation
  - 0 = Lane numbers reversed.
- **CFG[3]: MSR Privacy Bit Feature**
  - 1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting
  - 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden
- **CFG[4]: eDP enable**
  - 1 = Disabled
  - 0 = Enabled
- **CFG[6:5]: PCI Express* Bifurcation:**
  - 00 = 1 x8, 2 x4 PCI Express*
  - 01 = reserved
  - 10 = 2 x8 PCI Express*
  - 11 = 1 x16 PCI Express*
- **CFG[19:7]:** Reserved configuration lanes. A test point may be placed on the board for these lands.



INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV A01
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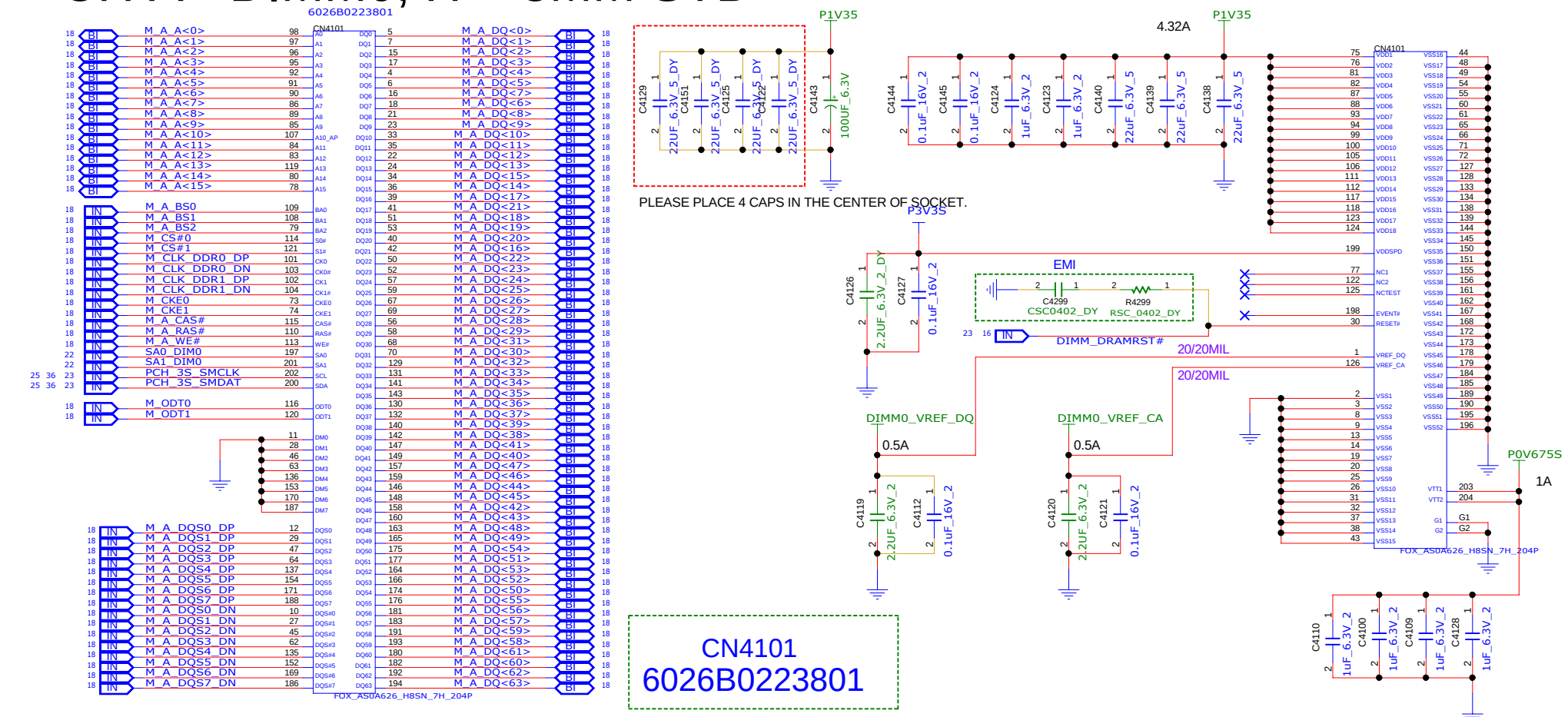
CH A - DIMM0, H = 8MM STD



INVENTEC	
TITLE	MODEL,PROJECT,FUNCTION Block Diagram
SIZE A3	CODE CS
DOC.NUMBER	1310xxxxx-0-0
REV	A01
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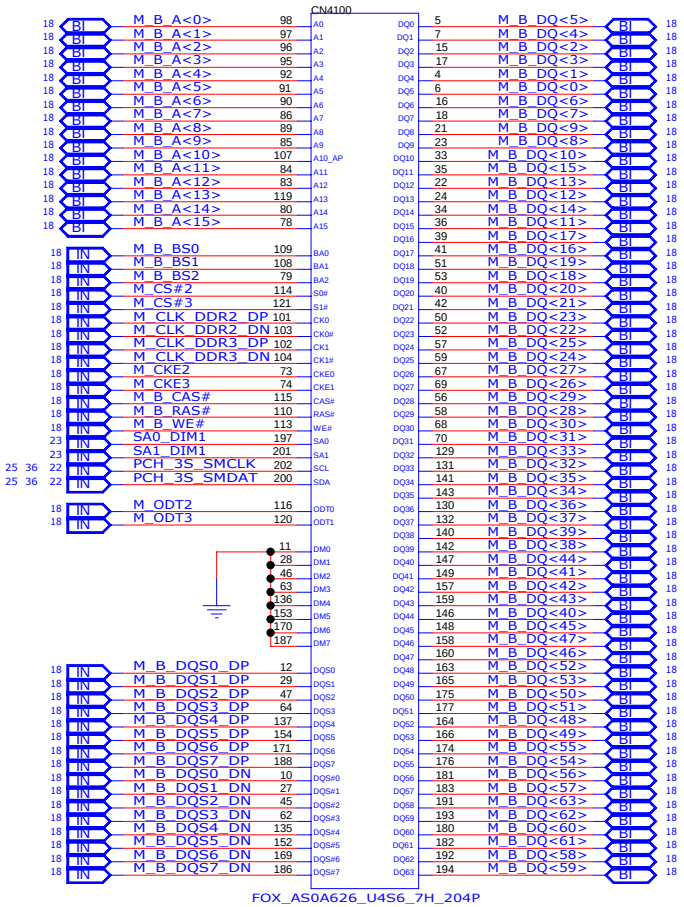
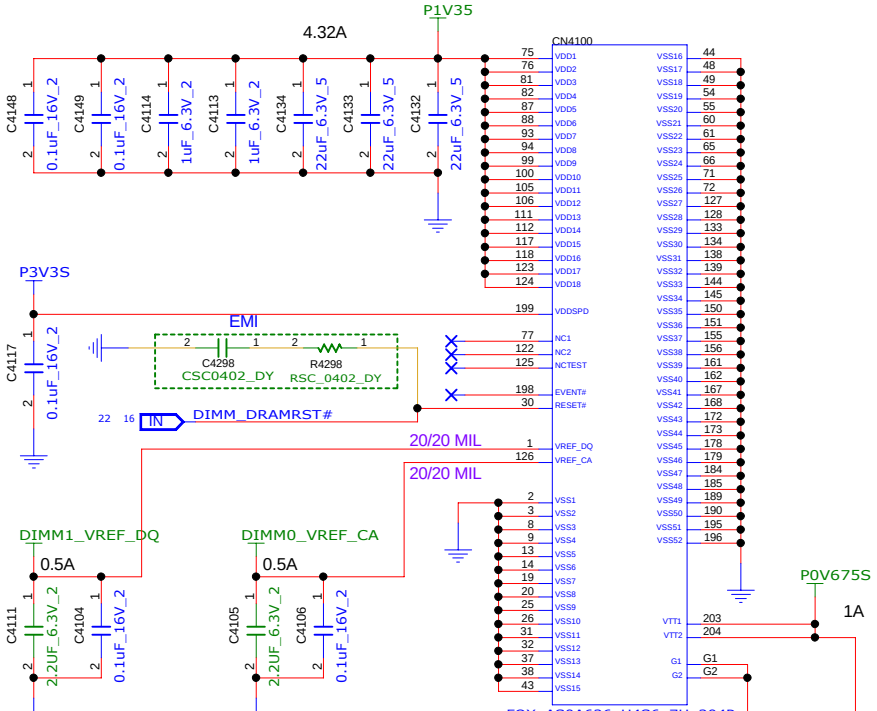
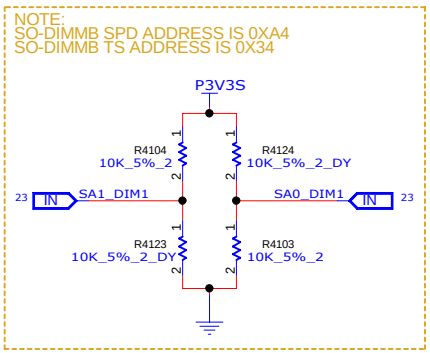
CH B - DIMM1, H = 4MM STD

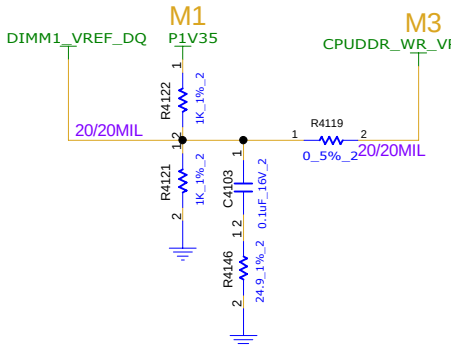
6026B0223701

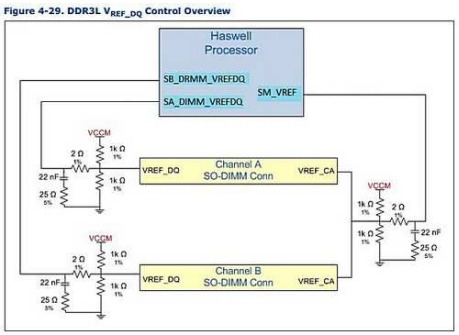


CN4100
6026B0223701









INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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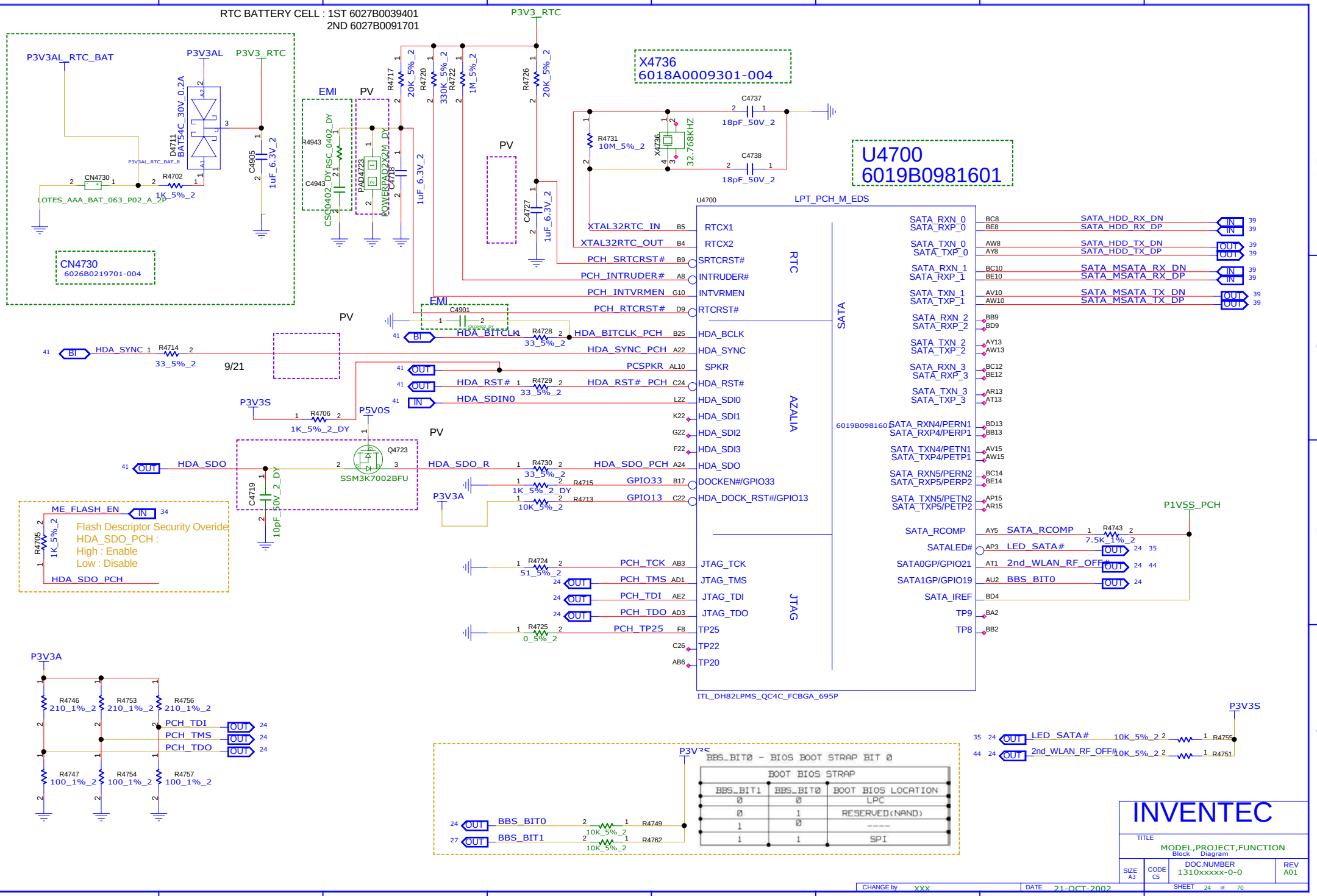
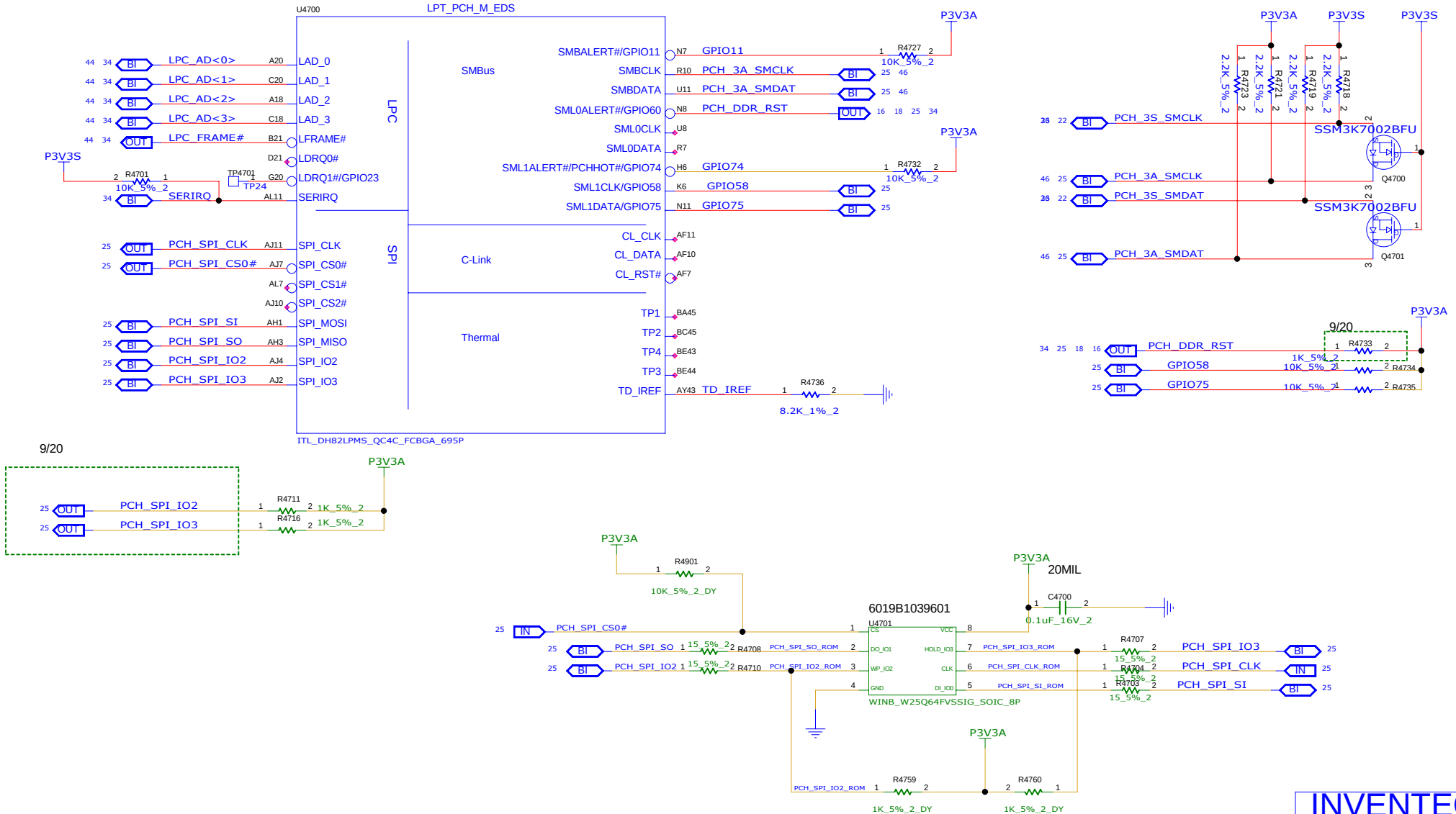
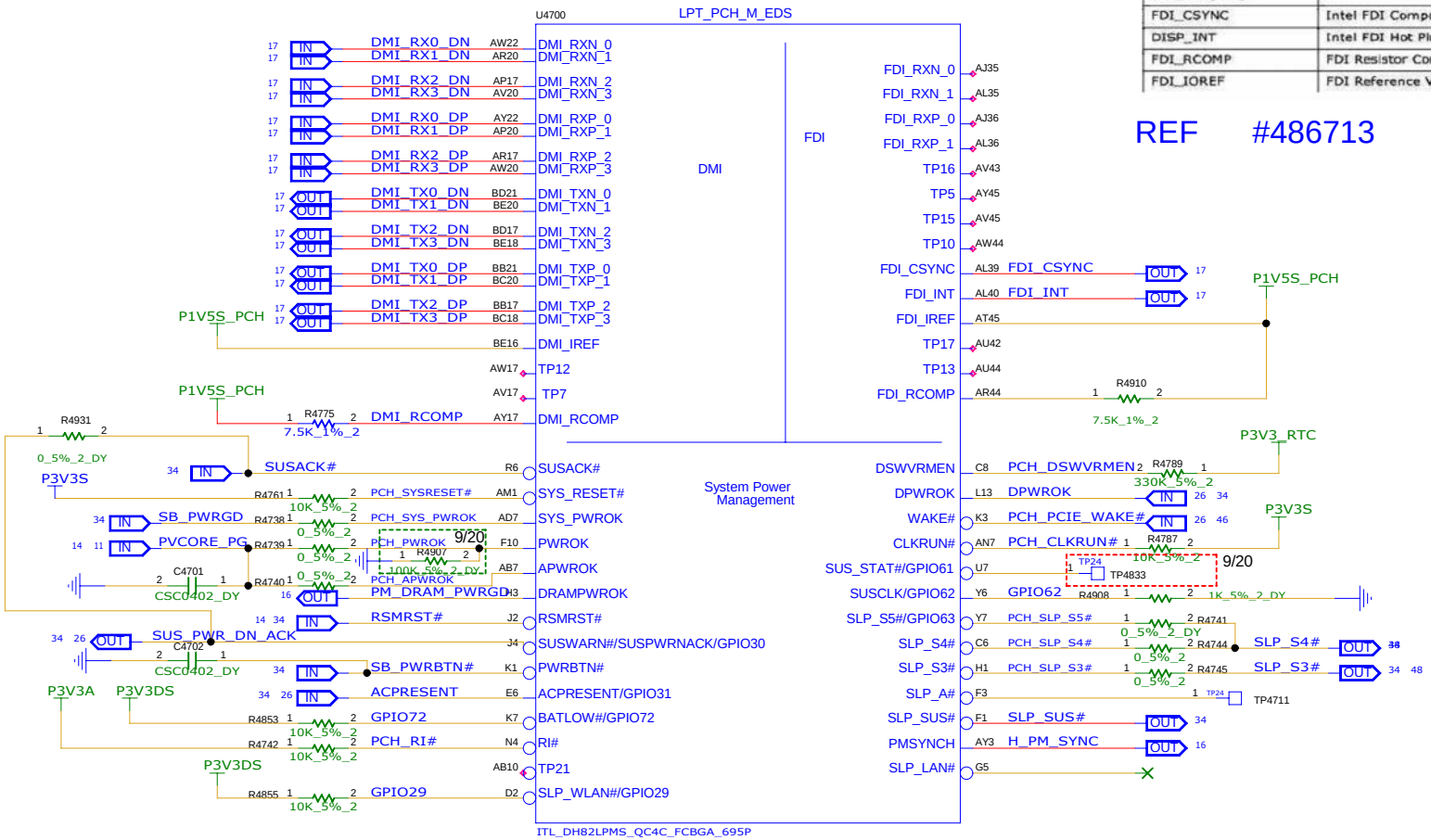


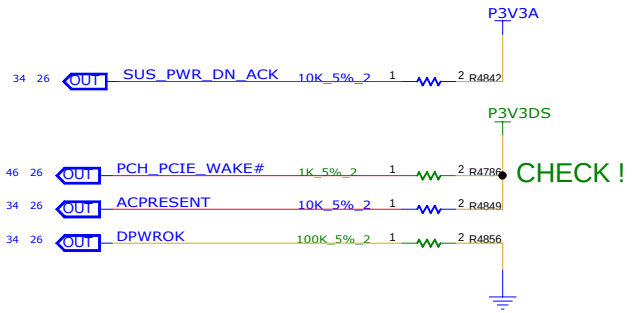


Signal	Description	Disable Guidelines
FDI_RXP[0:1] FDI_RXN[0:1]	Intel FDI Receive Differential Pair on PCH	Float
FDI_TXP[0:1] FDI_TXN[0:1]	Intel FDI Transmit Differential Pair on Processor	Float
FDI_CSYNC	Intel FDI Composite Sync	Connect to Processor and PCH
DISP_INT	Intel FDI Hot Plug Interrupt	Connect to Processor and PCH
FDI_RCOMP	FDI Resistor Compensation	Float
FDI_IOREF	FDI Reference Voltage	Float

REF #486713 INTEL SBY DG V1.0



power rail ->DSW :
SLP_A#
SLP_S3#
SLP_S4#
SLP_SUS#
SLP_LAN#
SLP_WLAN#/GPIO29
GPIO27
PWRBTN#
WAKE#
ACPRESENT/GPIO31
BATTLOW#/GPIO72
VCCDSW3_3
LAN_PHY_PWR_CTRL/GPIO12



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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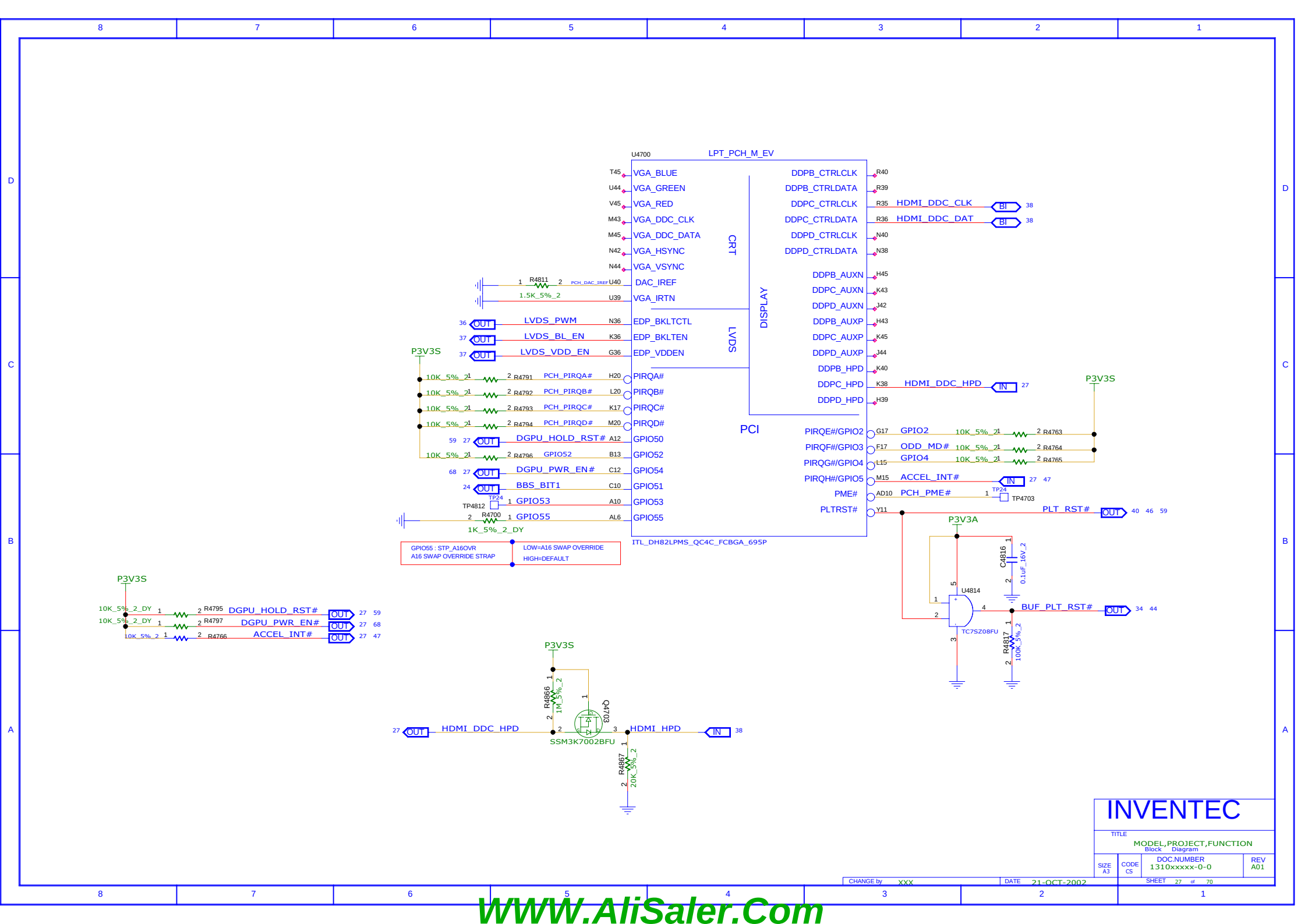

TITLE	MODEL,PROJECT,FUNCTION
	Block Diagram
SIZE A3	CODE CS
DOC.NUMBER	1310xxxxx-0-0
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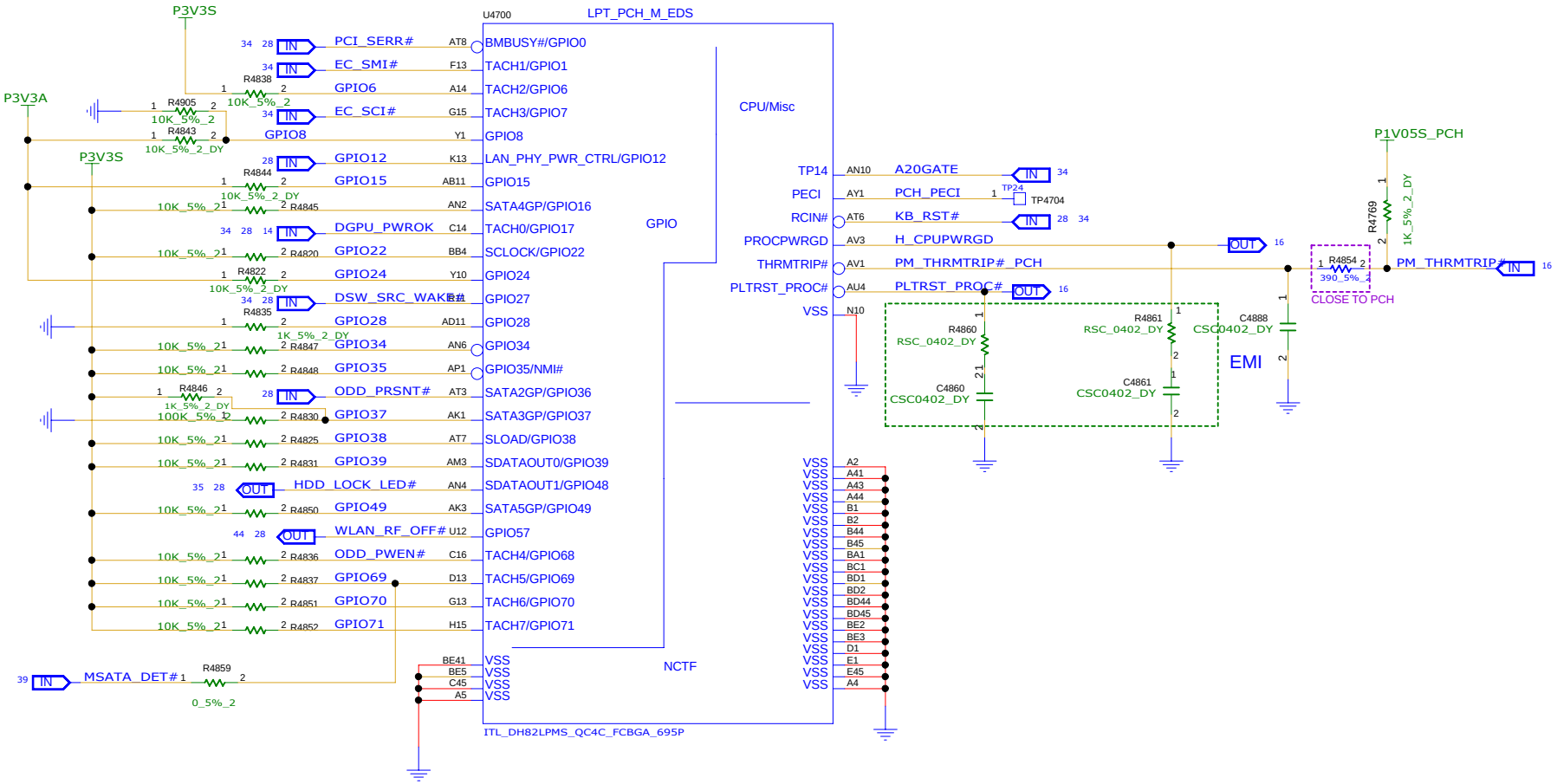
INVENTEC

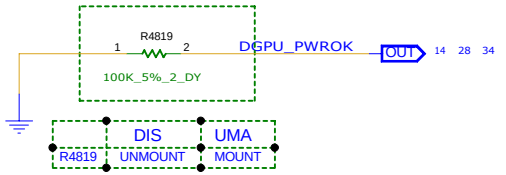
GPIO28

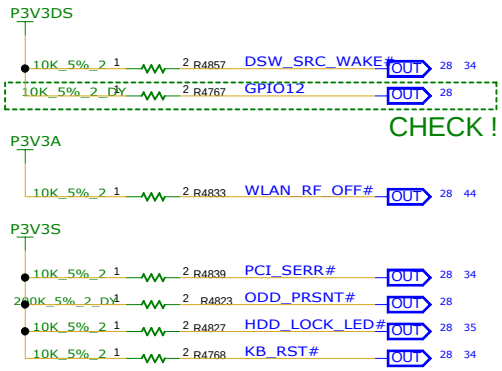
THE PIN REQUIRES GLITCH-FREE OUTPUT POWER SEQUENCE.
THE PAD SHOULD ONLY BE PULLED LOW
MOMENTARY
WHEN THE CORRESPONDING BUFFER POWER SUPPLY IS NOT STABLE.



GPIO36	RSVD	Rising edge of PWROK	This signal has a weak internal pull-down. **NOTE:** The internal pull-down is disabled after PLTRST# deasserts.
SATA3GP/GPIO37	TLS Confidentiality	Rising edge of PWROK pin	Low = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel ME Crypto TLS cipher suite with confidentiality This signal has a weak internal pull-down. **NOTES:** 1. A strong pull-up may be needed for GPIO functionality 2. This signal must be pulled up to support Intel AMT with TLS. Intel ME configuration parameters also need to be set correctly to enable TLS.

UMA





INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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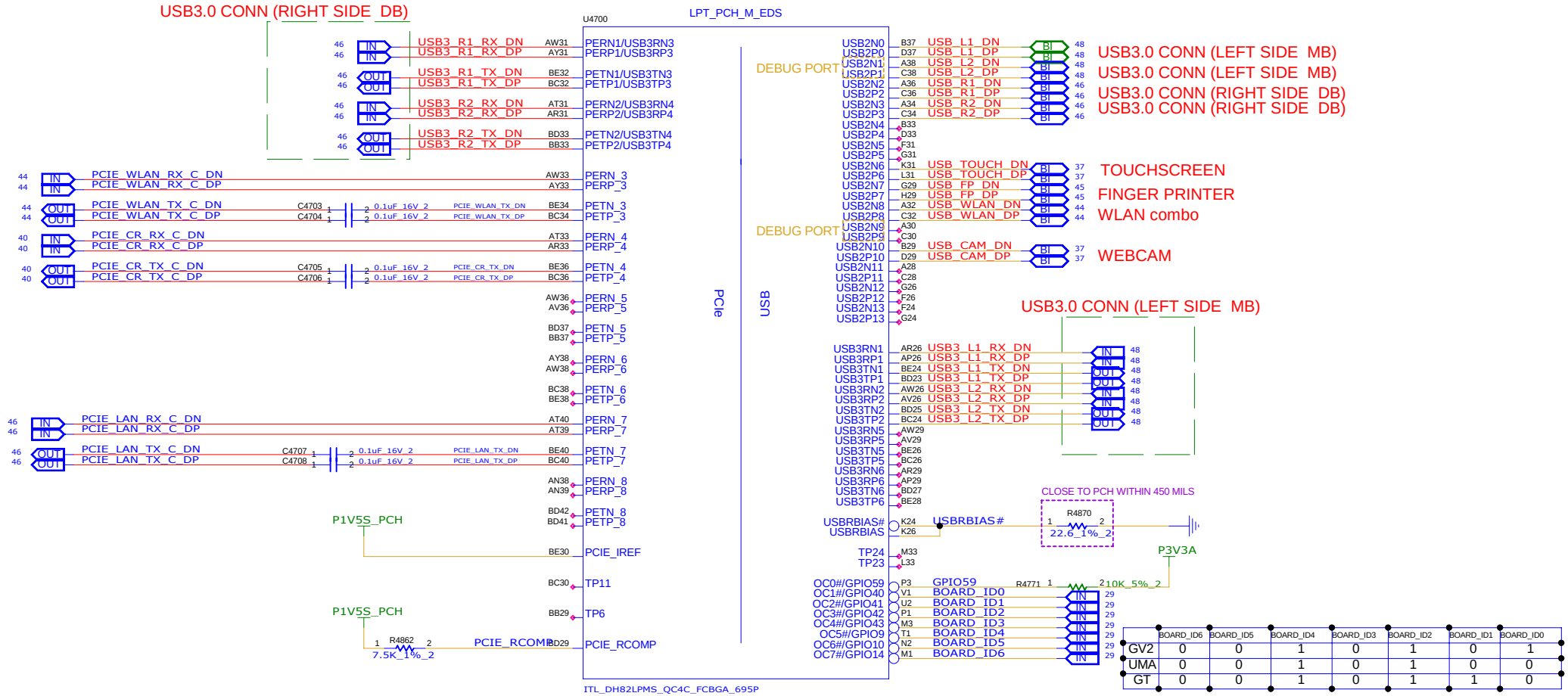
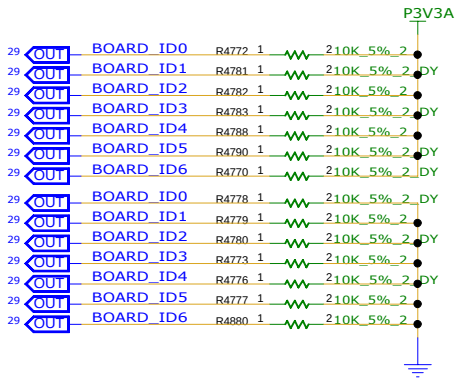


	BOARD_ID6	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
GV2	0	0	1	0	1	0	1
UMA	0	0	1	0	1	0	0
GT	0	0	1	0	1	1	0

Table 1-5. Mobile Lynx Point SKUs Flexible I/O Map

SKU	High Speed I/O Ports																	
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14	Port 15	Port 16	Port 17	Port 18
QM87	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 5	USB 3.0 Port 6	USB 3.0 Port 3 / PCIe* Port 1	USB 3.0 Port 4 / PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 6Gb/s Port 4 / PCIe* Port 1	SATA 6Gb/s Port 5 / PCIe* Port 2	SATA 6Gb/s Port 0	SATA 6Gb/s Port 1	SATA 3Gb/s Port 2	SATA 3Gb/s Port 3
HM87	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 5	USB 3.0 Port 6	USB 3.0 Port 3 / PCIe* Port 1	USB 3.0 Port 4 / PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 6Gb/s Port 4 / PCIe* Port 1	SATA 6Gb/s Port 5 / PCIe* Port 2	SATA 6Gb/s Port 0	SATA 6Gb/s Port 1	SATA 3Gb/s Port 2	SATA 3Gb/s Port 3
HM86	USB 3.0 Port 1	USB 3.0 Port 2	NA	NA	USB 3.0 Port 3 / PCIe* Port 1	USB 3.0 Port 4 / PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 6Gb/s Port 4	SATA 6Gb/s Port 5	SATA 3Gb/s Port 0	NA	SATA 3Gb/s Port 2	NA



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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SUK_0606

UMA DELETE

CLOCK SIGNAL

U4700 LPT_PCH_M_EDS

ITL_DH82LPMS_QC4C_FCBGA_695P

BUILD ID

	BUILD_ID1	BUILD_ID0
DB	0	0
SI	0	1
PV	1	0
MV	1	1

EMI

C4902, C4903, C4904

DGPU_PRSNT# :
UMA : Pull high
DIS : Pull down

X4928
6018B0060301

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3 | CODE CS | DOC.NUMBER 1310xxxxx-0-0 | REV A01

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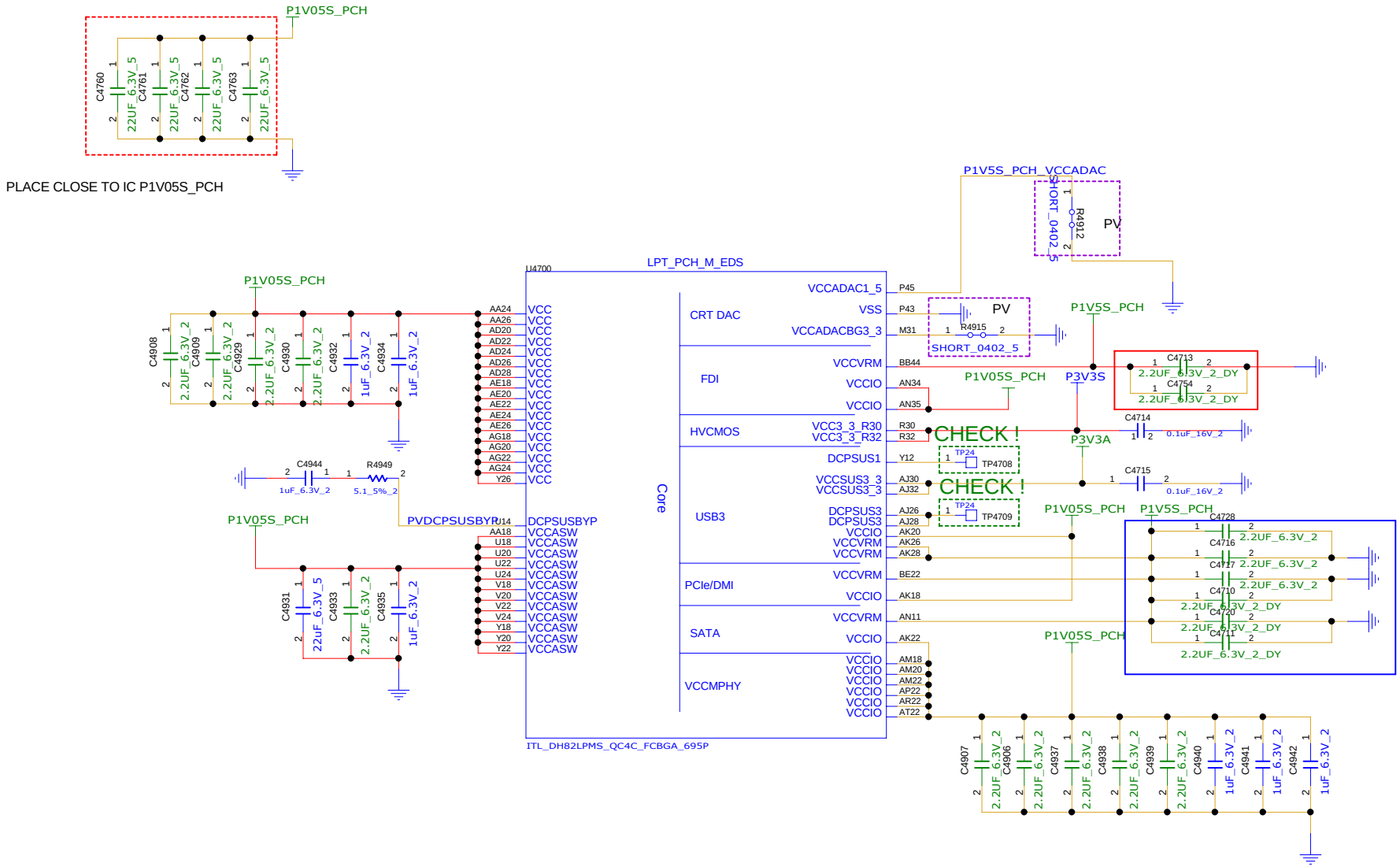
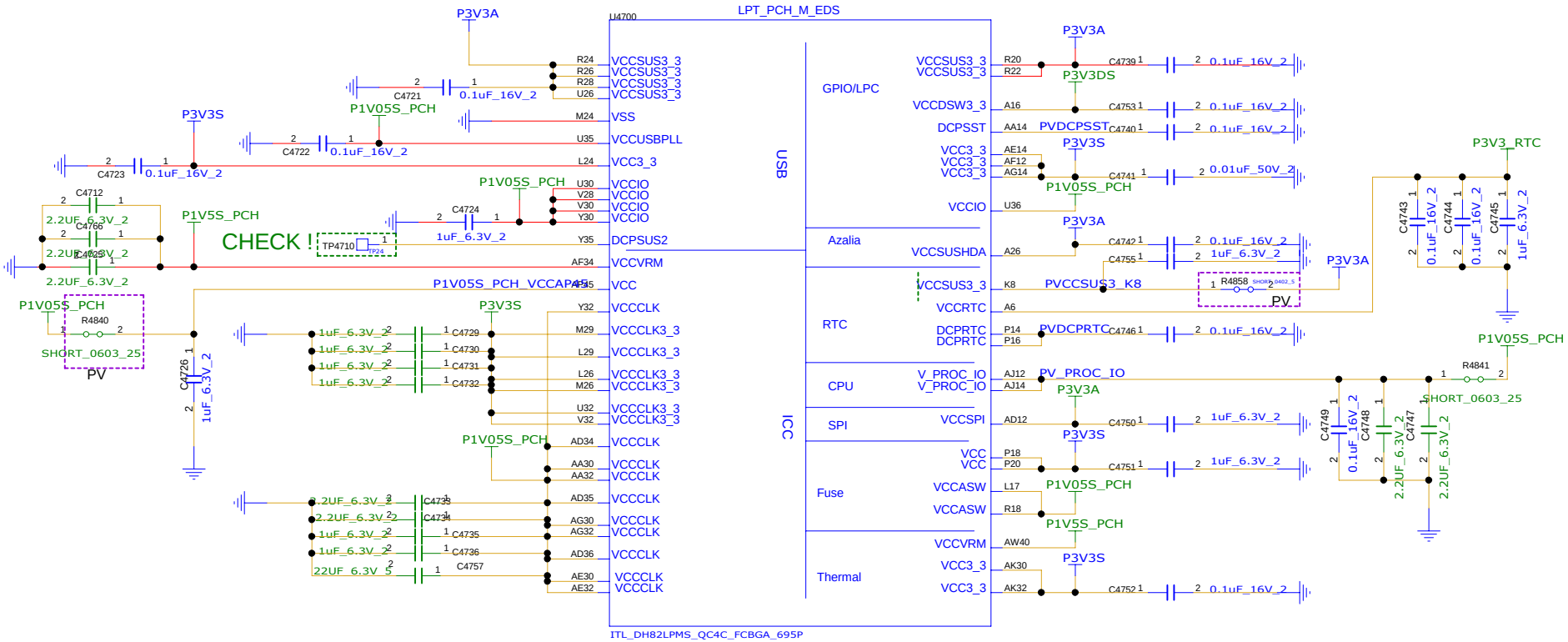
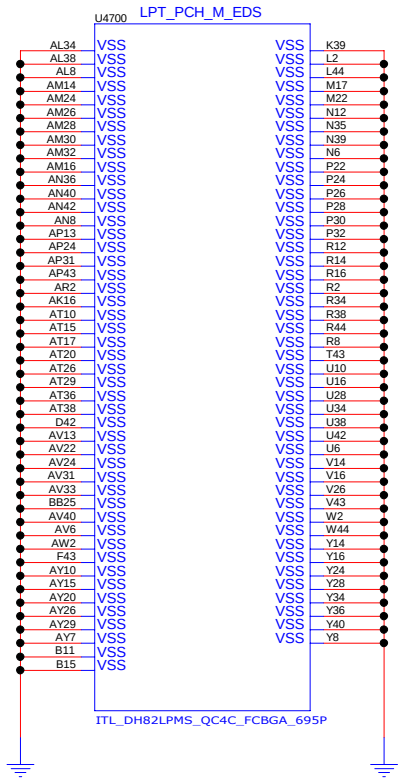


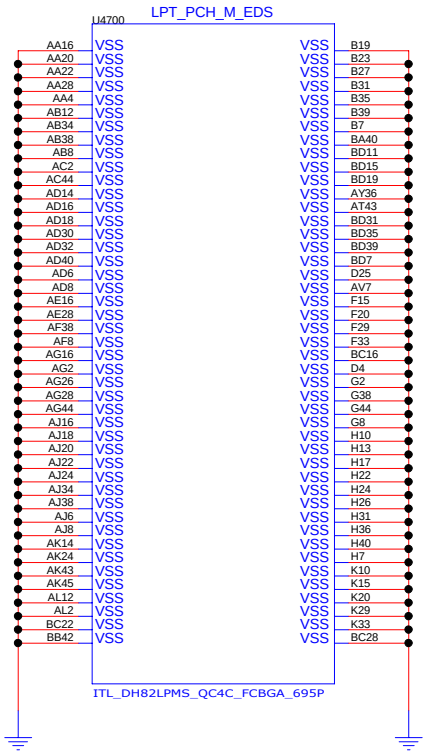
REF INTEL SBY DG #486713 V1.0

V3.3SS (3.3V)		USB3: AJ30, AJ32
		USB2: R24, R26, R28, U26
		Sus: R20, R22
		AZALIA: A26
		RTC: K8



INVENTEC		
TITLE: MODEL,PROJECT,FUNCTION (Block Diagram)		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0 / REV A01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 32 of 70





INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

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A3	CS	1310xxxxx-0-0	A01

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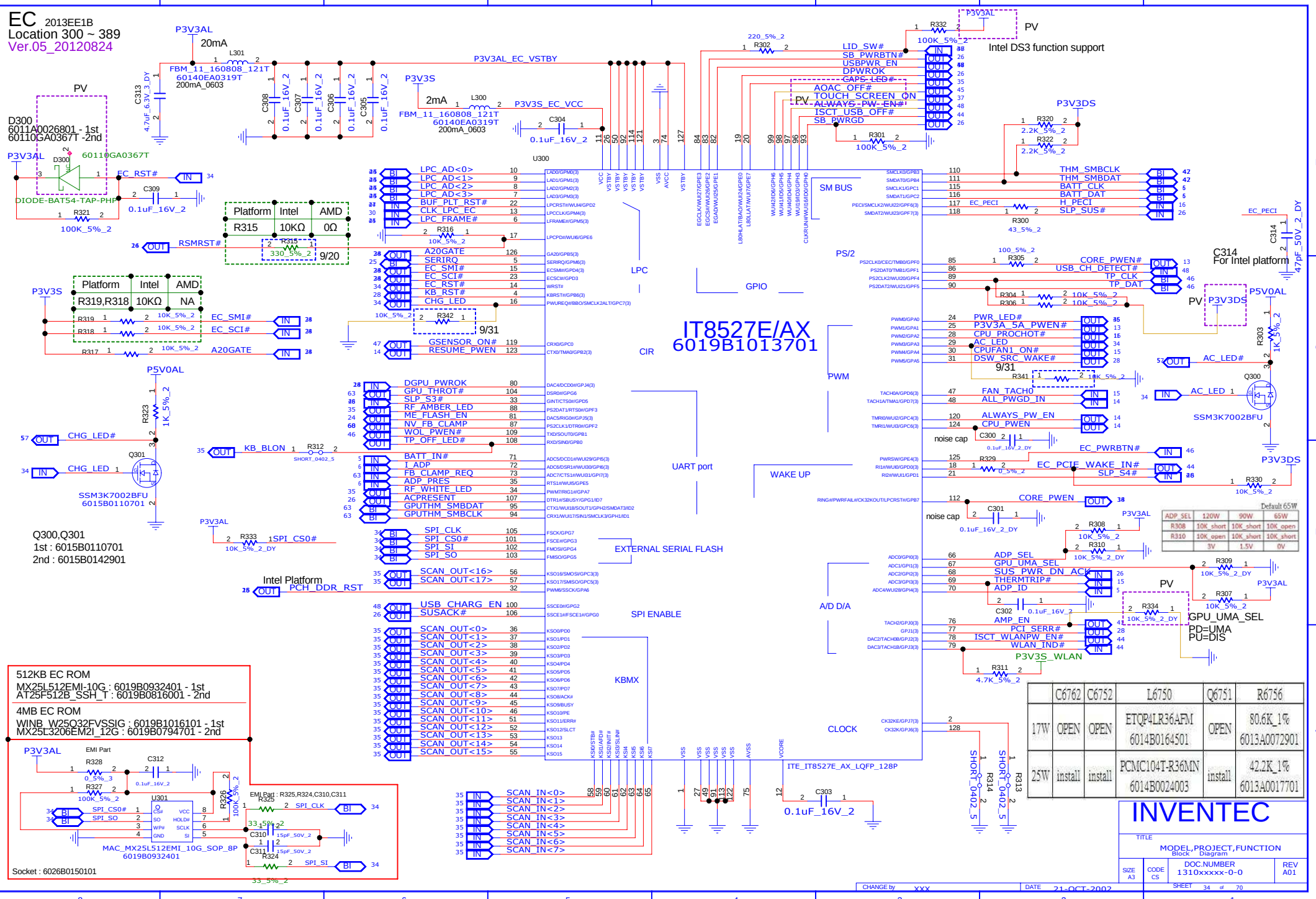
EC 2013EE1B

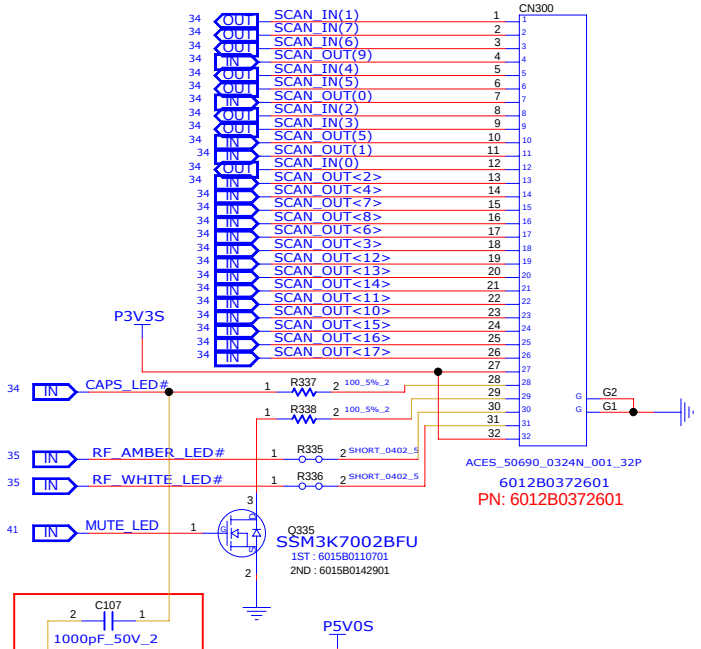
Location 300 ~ 389

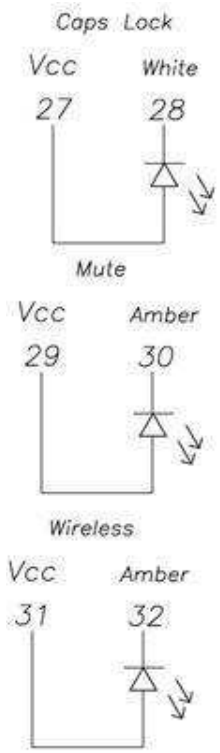
Ver.05_20120824



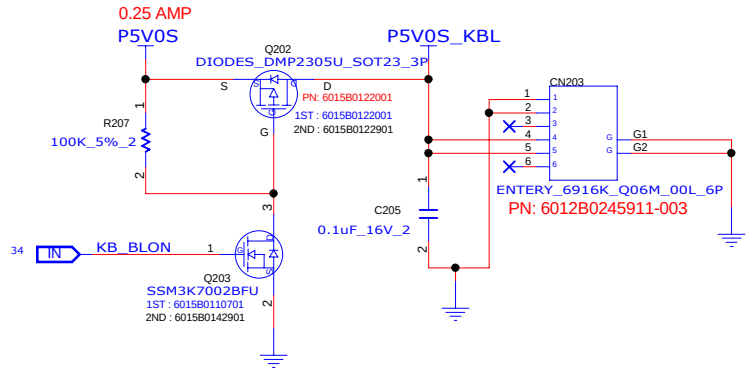
CONNECTOR KEY BOARD 200~299

KEYBOARD CONN(32 PIN)



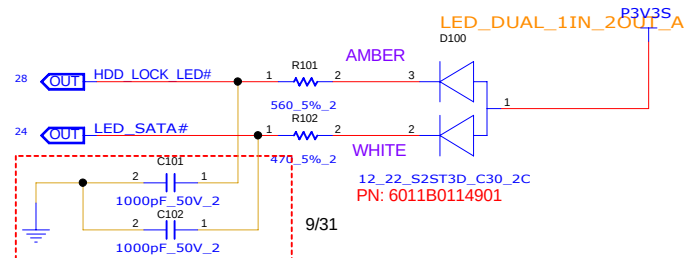


KEYBOARD BACKLIGHT



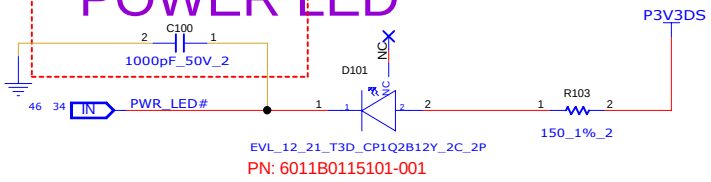
LED 100~199

HDD LED



9/31

POWER LED



INVENTEC			
TITLE: MODEL,PROJECT,FUNCTION KB_CONN & LED			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV A01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 35 of 70	

Location 3400~3499
Ver.02_20120824

P3V3S_DVDD33

U3400 ON_CAT24C64YI_GT3_TSSOP_8P_DY

R3427 0_5%_2_DY EDP_TRAN_EDID_CLK

R3434 0_5%_2_DY EDP_TRAN_EDID_DAT

CAT24C64Y I (8KBYTE) 6019B1016301

RESERVED FOR RTD2136R SERIES DEBUG

P3V3S_DVDD33 R3423 4.7K_5%_2 R3424 4.7K_5%_2

EDP_TRAN_EDID_CLK EDP_TRAN_EDID_DAT

P3V3S_DVDD33 R3428 2.1M_5%_2_DY EDP_TRAN_AUX_DP

R3429 2.1M_5%_2_DY EDP_TRAN_AUX_DN

ENTIRE TRACE OF PANEL VCC SHOULD BE WIDER THAN 80-MIL

P3V3S PAD3400 POWERPAD1x1m P3V3S_DVDD33 C3400 0.1UF_16V_2 C3401 10UF_6.3V_3

P3V3S 6014B0041601 L3402 BLM18PG121SN1 P3V3S_AVDD33 C3415 0.1UF_16V_2 C3416 10UF_6.3V_3

SWR MODE

SHOULD CHANGE TO TAIYO YUDEN NRH3010T-2R2MN

IN SWR_LX1 L3401 VCCK_V12 OUT

TAITECH_SWF2520CF-2R2M-R15 C3414 10UF_6.3V_3 C3413 0.1UF_16V_2

MODE_CFG1 (PIN 48)	MODE_CFG0(PIN 47) = 0	MODE_CFG0(PIN 47) = 1
0	X	EP MODE
1	ROM ONLY MODE	EEPROM MODE

P3V3S_DVDD33 R3414 4.7K_5%_2 R3435 4.7K_5%_2_DY MODE_CFG0 MODE_CFG1

R3415 4.7K_5%_2_DY R3416 4.7K_5%_2

FOR EDP ONLY

LVDS_PWM R3425 0_5%_2_DY LVDS_PWM_R

NB_EDP_TX1_DP R3412 0_5%_2_DY NB_EDP_TX1_R_DP

NB_EDP_TX1_DN R3409 0_5%_2_DY NB_EDP_TX1_R_DN

NB_EDP_TX0_DP R3403 0_5%_2_DY NB_EDP_TX0_R_DP

NB_EDP_TX0_DN R3400 0_5%_2_DY NB_EDP_TX0_R_DN

NB_EDP_AUX_DP R3404 0_5%_2_DY NB_EDP_AUX_R_DP

NB_EDP_AUX_DN R3407 0_5%_2_DY NB_EDP_AUX_R_DN

LVDS_DDC_DAT R3418 0_5%_2 EDP_TRAN_LCD_BKEN

LVDS_DDC_CLK R3419 0_5%_2 EDP_TRAN_EDID_DAT

EDP_TRAN_EDID_CLK

MODE_CFG0

MODE_CFG1

P3V3S_AVDD33 C3417 0.1UF_16V_2

R3417 100K_5%_2 EDP_TRAN_HPD R3432 1K_5%_2

NB_EDP_AUX_DN C3406 0.1UF_16V_2 EDP_TRAN_AUX_DN

NB_EDP_AUX_DP C3407 0.1UF_16V_2 EDP_TRAN_AUX_DP

NB_EDP_TX0_DP C3402 0.1UF_16V_2 EDP_TRAN_TX0_DP

NB_EDP_TX0_DN C3404 0.1UF_16V_2 EDP_TRAN_TX0_DN

NB_EDP_TX1_DP C3403 0.1UF_16V_2 EDP_TRAN_TX1_DP

NB_EDP_TX1_DN C3405 0.1UF_16V_2 EDP_TRAN_TX1_DN

VCCK_V12 R3413 12K_1%_2 C3408 0.1UF_16V_2

U3401 RTD2136R REA_RTD2136R_CG_QFN_48P

EPAD_GND MODE_CFG1 MODE_CFG0 MICSCL MICSDA BL_EN VCCK TXO0- TXO0+ TXO1- TXO1+ TXO2- TXO2+

DP_HPD TEST_MODE AUX_CH_N AUX_CH_P DP_V33 DP_GND LANE0_P LANE0_N LANE1_P LANE1_N DP_V12 DP_REXT

CICSCL CICSDA SWR_VCCK/LDO_VCCK GND SWR_LX/LDO_FB SWR_VDD/LDO_VDD PWMOUT PANEL_VCC PWMN PVCC TXE3+ TXE3-

TXOC- TXOC+ TXO3- TXO3+ TXE0- TXE0+ TXE1- TXE1+ TXE2- TXE2+ TXEC- TXEC+

C3411 0.1UF_16V_2

VCCK_V12 LVDSA_D0_DN LVDSA_D0_DP LVDSA_D1_DN LVDSA_D1_DP LVDSA_D2_DN LVDSA_D2_DP

LVDSA_CLK_DN LVDSA_CLK_DP

LVDSB_D0_DN LVDSB_D0_DP LVDSB_D1_DN LVDSB_D1_DP LVDSB_D2_DN LVDSB_D2_DP LVDSB_CLK_DN LVDSB_CLK_DP

P3V3S_DVDD33 9/20 R3421 4.7K_5%_2_DY R3422 4.7K_5%_2_DY

PCH_3S_SMCLK PCH_3S_SMDAT VCCK_V12 SWR_LX

R3433 0_5%_2

LVDS_PWM P3V3S_LCDVDD_EDP LVDS_PWM_R

P3V3S_DVDD33 C3409 0.1UF_16V_2 C3410 22UF_6.3V_5

R3431 100K_5%_2_DY R3430 1K_5%_2_DY

P3V3S_DVDD33 C3412 0.1UF_16V_2

ENTIRE TRACE OF PANEL VCC SHOULD BE WIDER THAN 80-MIL

INVENTEC

TITLE MODEL,PROJECT,FUNCTION Block Diagram

SIZE A3 | CODE CS | DOC.NUMBER 1310xxxxx-0-0 | REV A01

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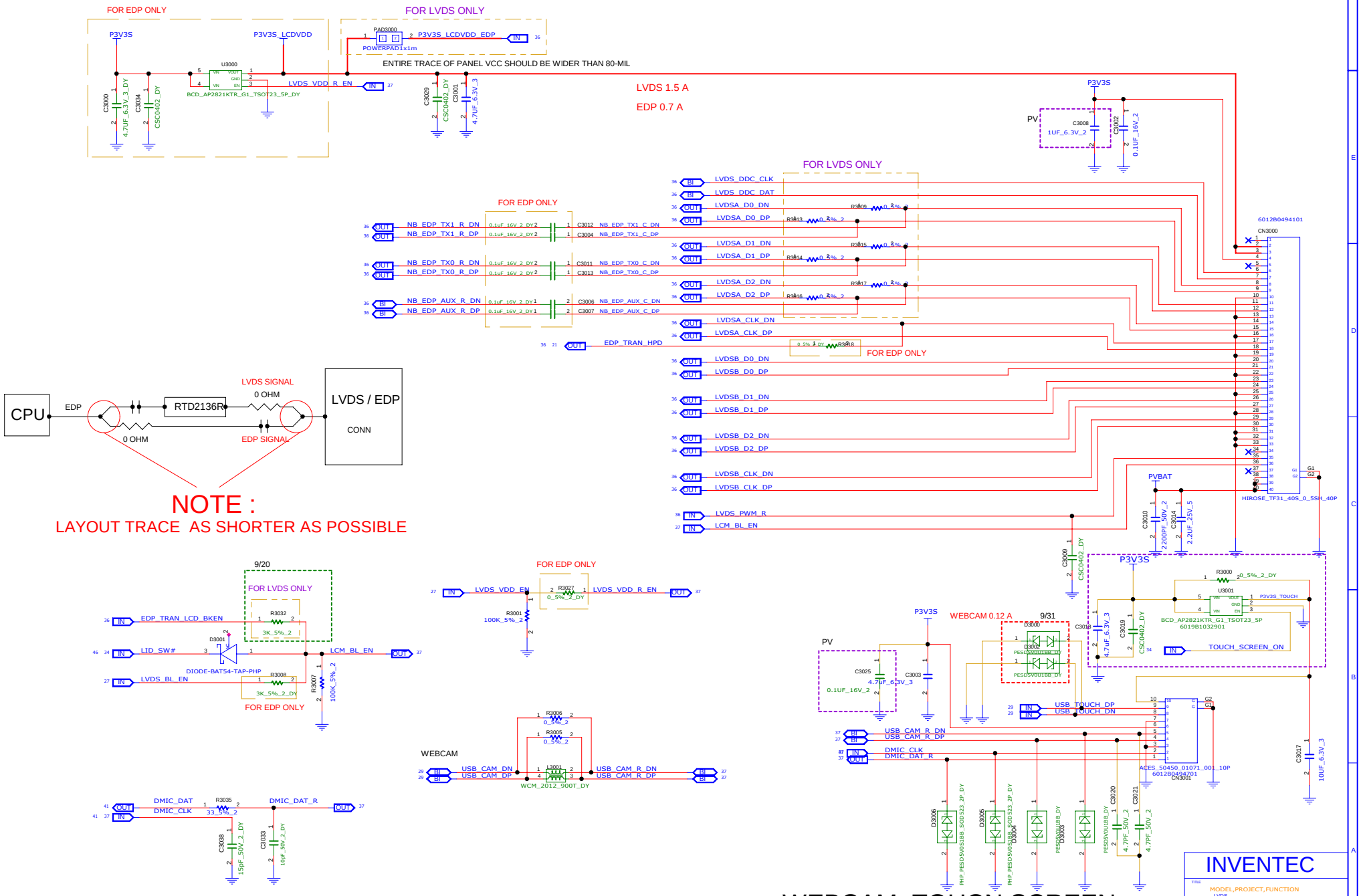
40 PIN LCM CONN FOR RTD2136R

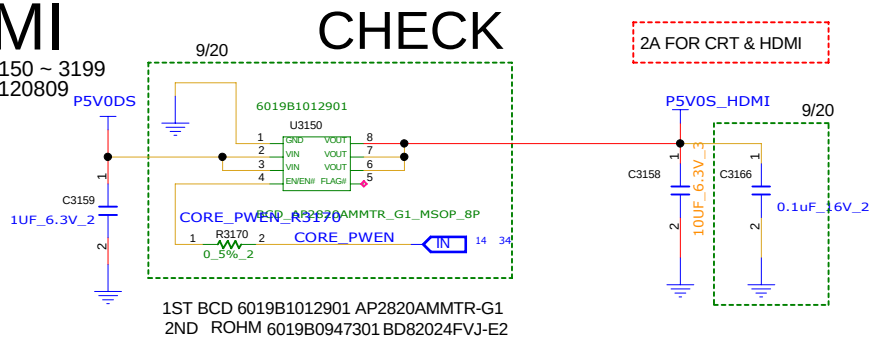
Location 3000~3049
Ver.02_20120824



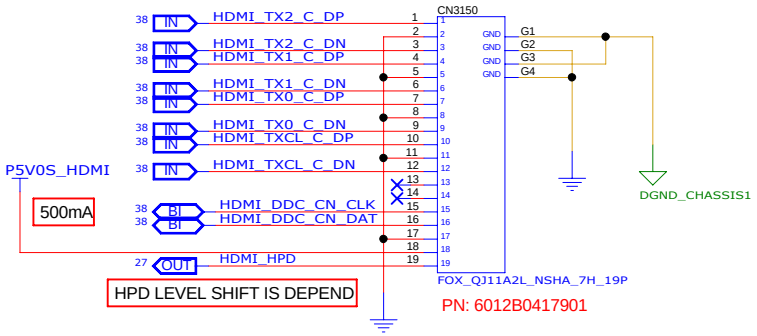
HDMI

Location 3150 ~ 3199
Ver.02_20120809

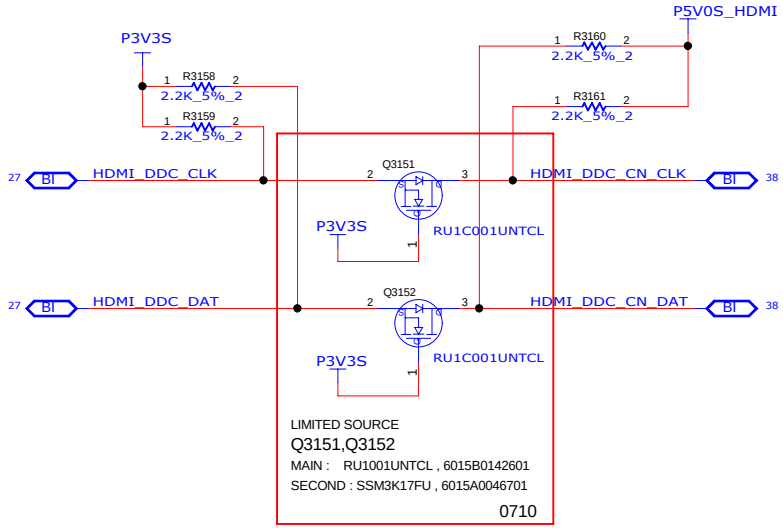
CHECK



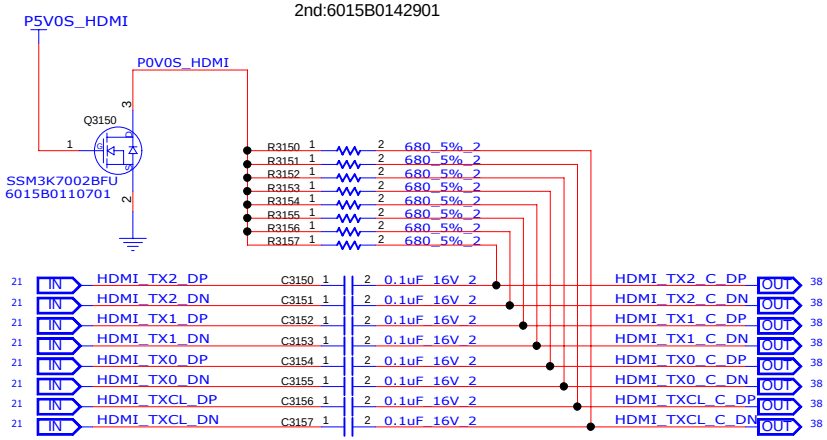
1ST BCD 6019B1012901 AP2820AMMTR-G1
2ND ROHM 6019B0947301 BD82024FVJ-E2



PN: 6012B0417901



Q3150
1st:6015B0110701
2nd:6015B0142901



Location	Part number	Factory	Manufacturer Part No	Marking
D300	1ST : 6011A0026801	DIODES	D-BAT54-7	KL1
	2nd : 60110GA0367T	NXP	BAT54	
Q300	1ST : 6015B0124601	NXP	2N7002P	LWx
Q301	2nd : 6015B0140901	DIODES	DMN65D8L-7	MM6
U301	1ST : 6019B0932401	MXIC	MX25L512EMI-10G	
512KB	2nd : 6019B0816001	ATMEL	AT25F512B-SSH-T	
U301	1ST : 6019B1016101	WINBOND	W25Q32FVSSIG	
4MB	2nd : 6019B0794701	MXIC	MX25L3206EM2I-12G	

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
HDMI CONN

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	A01

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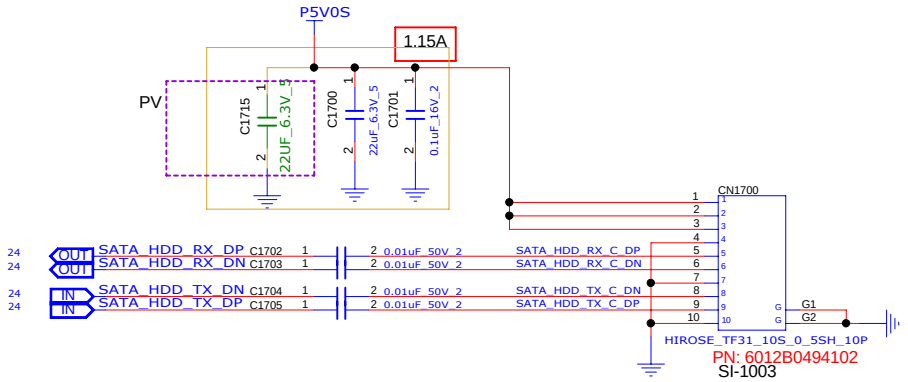
SATA HDD
Location 1700 ~ 1749

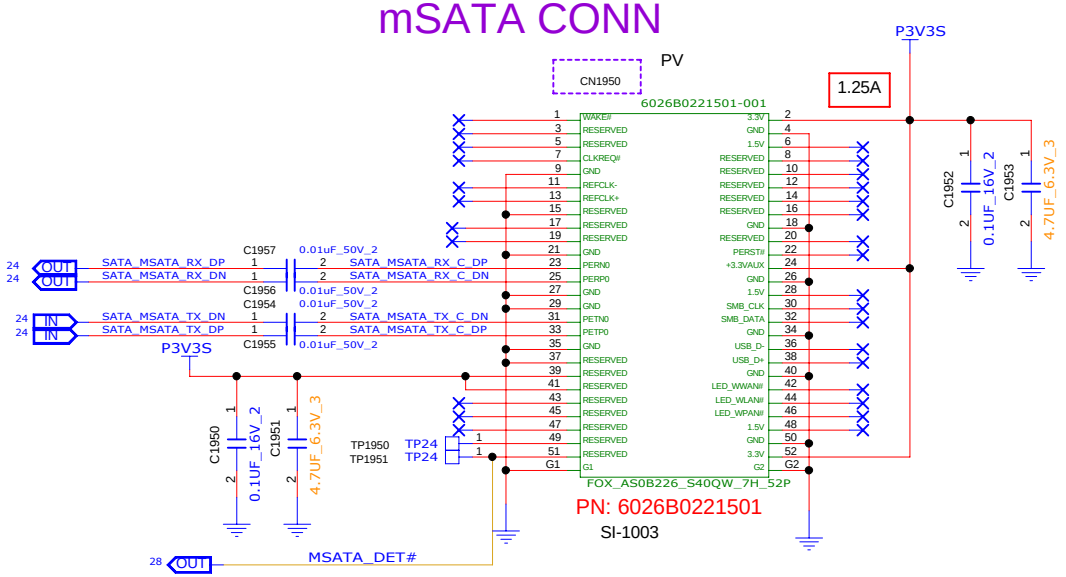
mSATA
Location 1950 ~ 1999

Ver.01_20120808

SATA HDD CABLE CONN on MB



mSATA CONN



INVENTEC

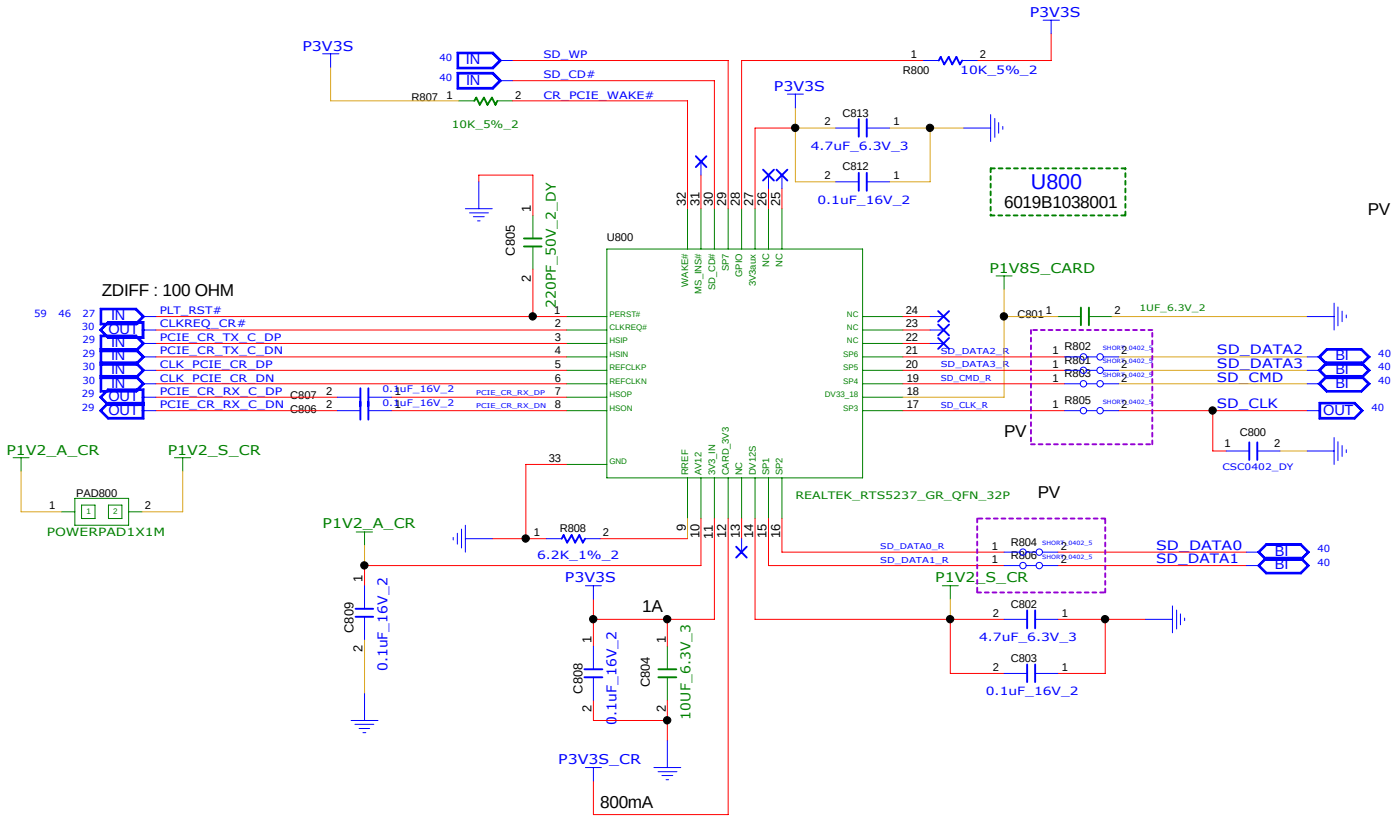
TITLE: MODEL,PROJECT,FUNCTION
SATA HDD & SATA ODD

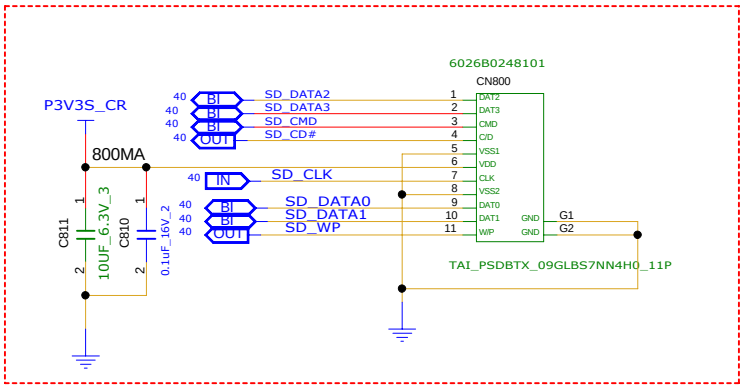
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	A01

CHANGE by XXX | DATE 21-OCT-2002 | SHEET 39 of 70

CARD READER
RTS5237

LOCATION: 800~899
VER_03 . 20120823





INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	A01

CHANGE by XXX | DATE 21-OCT-2002 | SHEET 40 of 70

AUDIO-1

CODEC

LOCATION: 500~549
VER.06_20120824

DVDD 0.025AMP
AVDD 0.06AMP
PVDD 0.01.3AMP

P5V0S
U501
BCD_AP2127K_4_75TRG1_SOT23_5P
PN: 6019B0668701
L501 BLM18PG600SN1D
0.06 AMP
P5V0S_AUDIO_AVDD
AGND_AUDIO

P3V3S
CLOSE TO PIN9
CLOSE TO PIN3
CLOSE TO PIN1

U500
PN:6019B0972801
IDT_92HD91B2X5NLGXWCX_QFN_48P

HDA_BITCLK
HDA_SDO
HDA_SYNC
HDA_SDIN0
HDA_RST#
HDA_SDIN0_R
NA

DMIC_CLK
DMIC_DAT

AMP_EN
D500
BAT54C_30V_0.2A
PN: 6011A0026803
MUTE_LED
AMP_EN_AU

SENSE_A
SENSE_B
MIC
VREFOUT_MIC
HP_L_AMP
HP_R_AMP
SPK_L
SPK_R
FRONT_SPK_OUT_L+
FRONT_SPK_OUT_L-
FRONT_SPK_OUT_R+
FRONT_SPK_OUT_R-
SUB_OUT
PCBEEP

CLOSS TO AUDIO
FRONT_SPK_OUT_R+
FRONT_SPK_OUT_R-
FRONT_SPK_OUT_L-
FRONT_SPK_OUT_L+
SI-1016 EMI
SI-1016 EMI

FRONT SPEAKER
6012B0069911
CN500
ACES_50224_0040N_001_4P

CLOSS TO AUDIO
PCSPKR
Q500
SSM3K7002BFU_DY

PAD500
POWERPAD_2_0610

PORT	DISCRIPTION	SENSE
A	MICROPHONE	SENSE_A
B	HEADPHONE	SENSE_A
C	NO USE	
D	FRONT SPKR	
E	NO USE	
F	REAR SPKR	

Default 65W

ADP_SEL	120W	90W	65W
R308	10K_short	10K_short	10K_open
R310	10K_open	10K_short	10K_short
	3V	1.5V	0V

CLOSE TO AUDIO CODEC

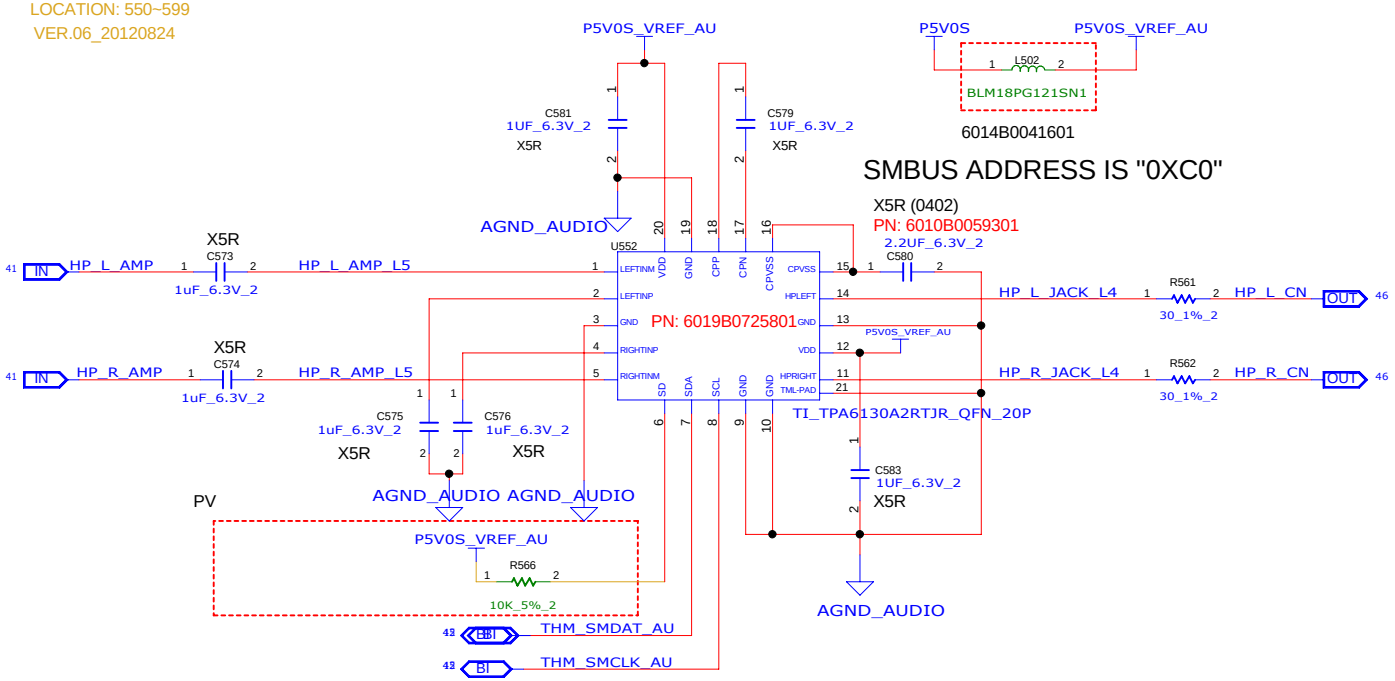
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram
SIZE A3 | CODE CS | DOC.NUMBER 1310xxxxx-0-0 | REV A01
CHANGE by XXX | DATE 21-OCT-2002 | SHEET 41 of 70

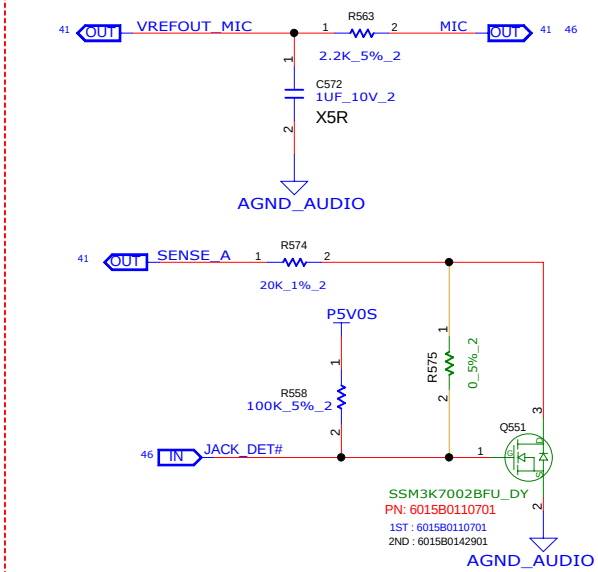
AUDIO-2

CODEC

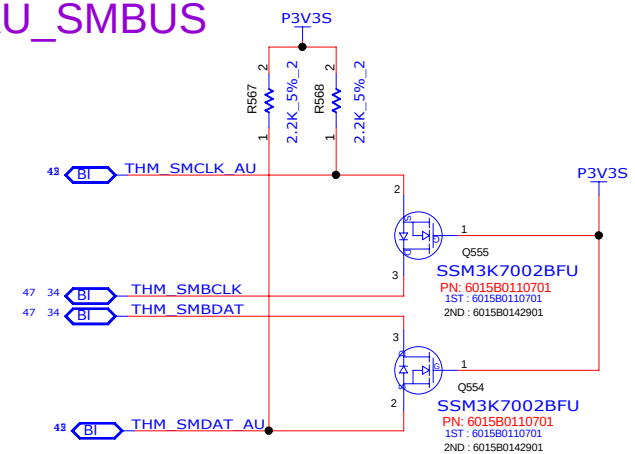
LOCATION: 550~599
VER.06_20120824



COMBO JACK



AU_SMBUS



Location	Part number	Factory	Manufacturer Part No	Marking
Q9401	1st : 6015B0122001	DIODES	DMP2305U	23P
	2nd : 6015B0122901	TOSHIBA	SSM3J327R	KFG
L9401	1st : 6014B0200401	TAI-TECH	SWF2520CF-2R2M-R15	
	2nd : 6014B0190301	CYNTEC	PHI25201B-2R2MS	
X9401	1st : 6018B0060301	EPSON	FA-238G	2500M
	2nd : 6018B0054701	TXC	7V25000014	T250

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3 | CODE CS | DOC.NUMBER 1310xxxxx-0-0 | REV A01

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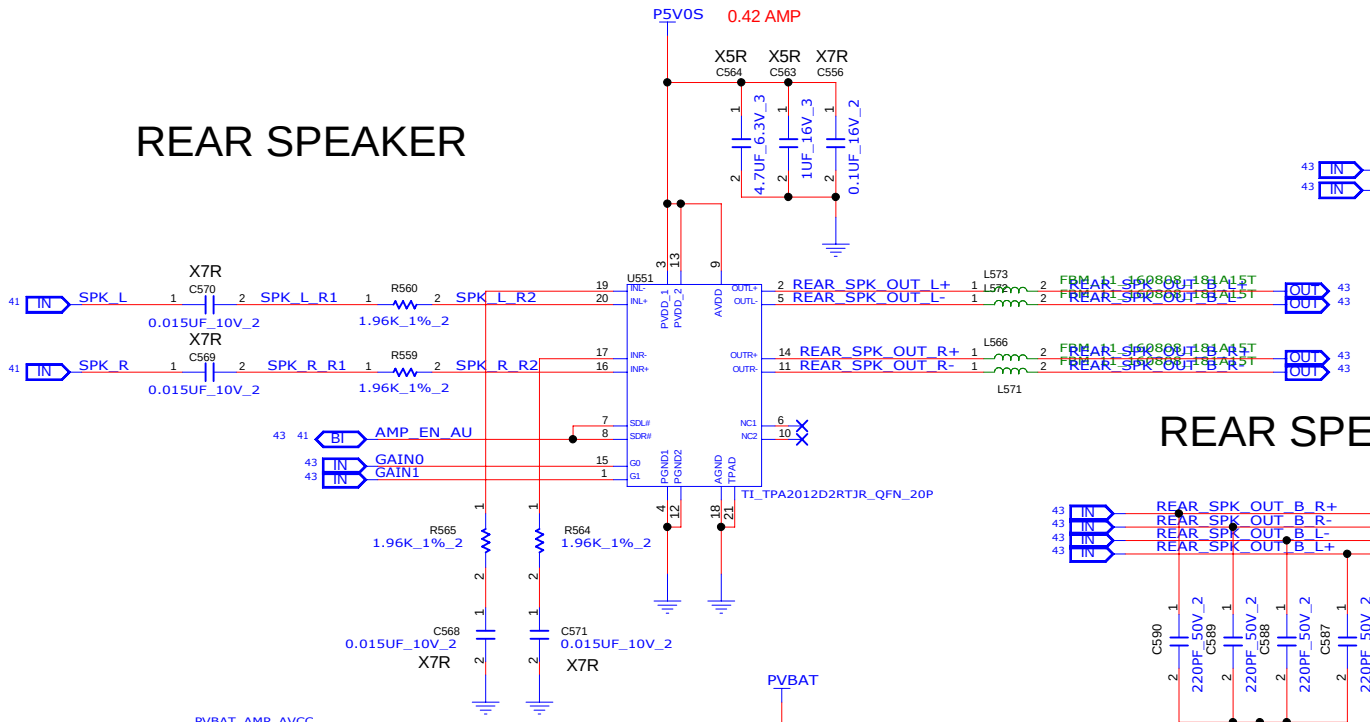
AUDIO (AMP) 550~599

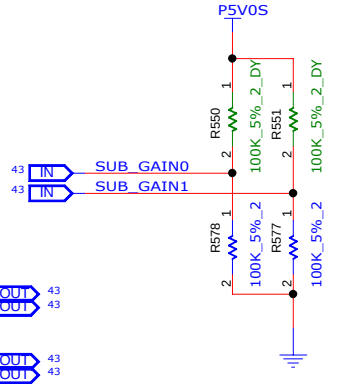
AUDIO-3

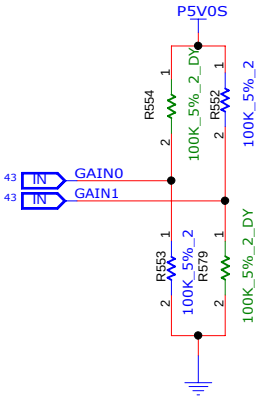
CODEC

LOCATION: 550~599
VER.06_20120824

REAR SPEAKER





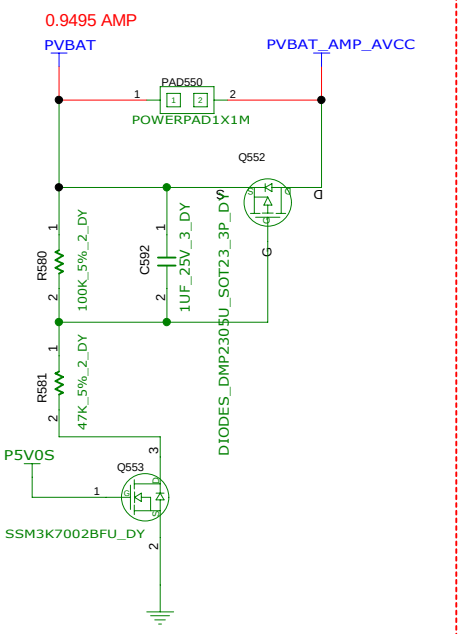


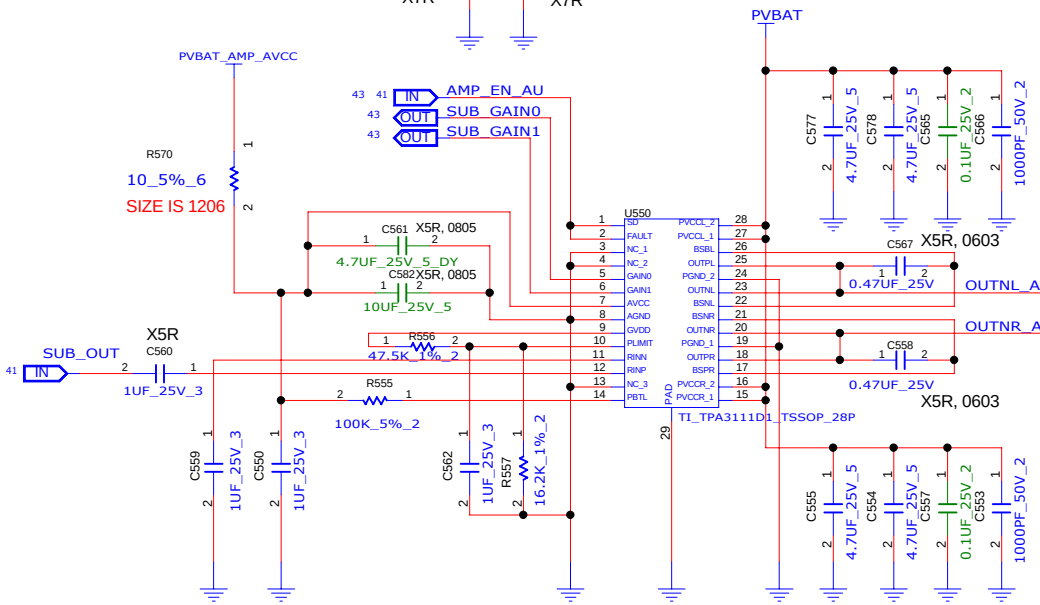
REAR SPEAKER

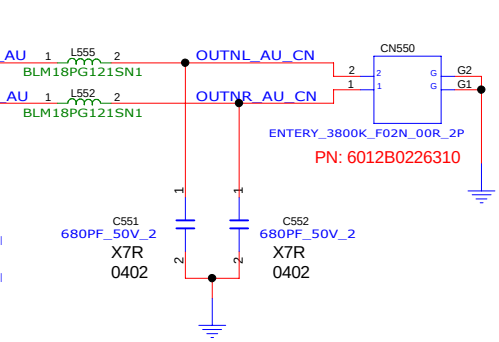
6012B0069911

SUBWOOFER

NA







TI TPA3111D1 (HP PART NUMBER HPA00836PWPR)

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	A01

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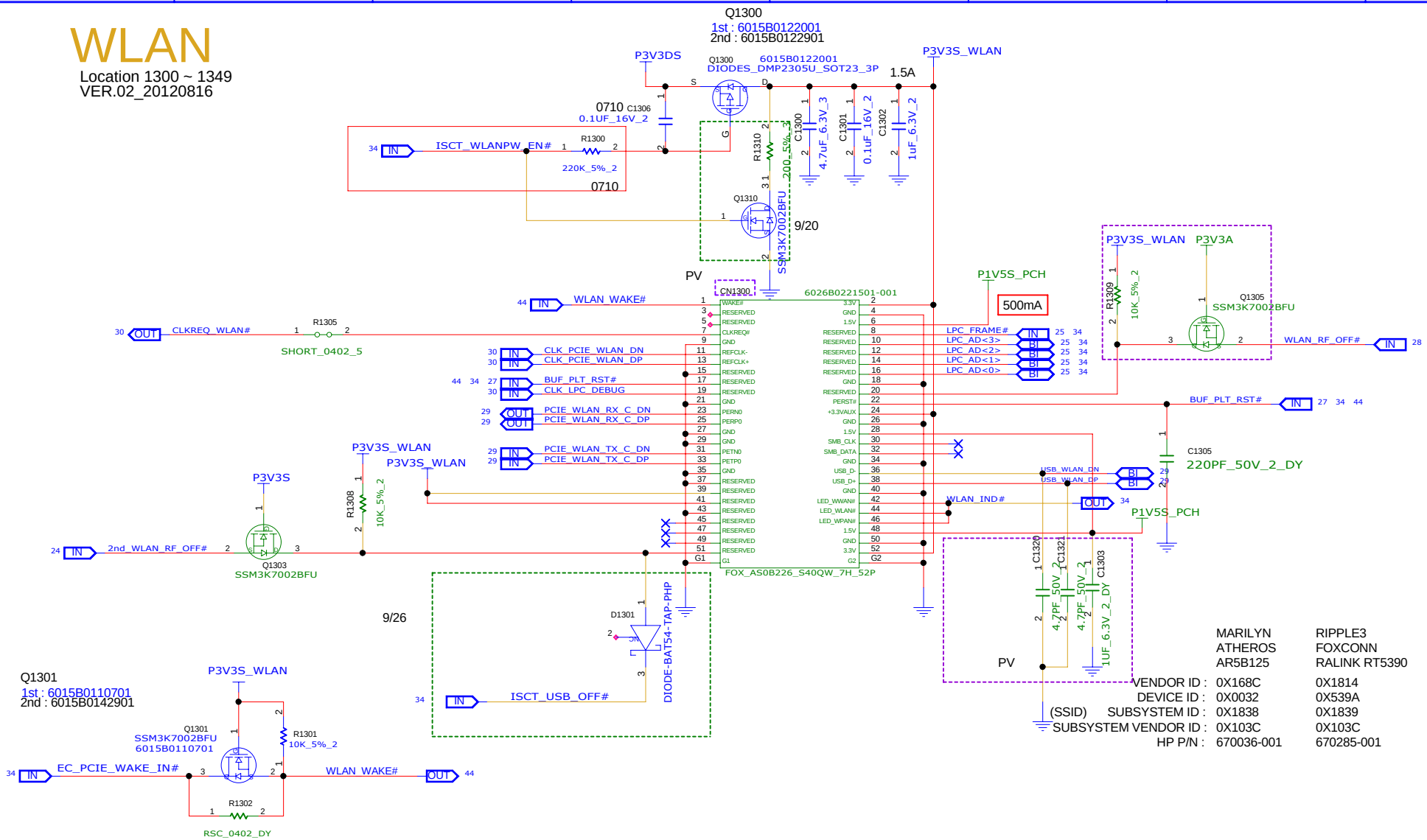
WLAN

Location 1300 ~ 1349
VER.02_20120816



	MARILYN	RIPPLE3
	ATHEROS	FOXCONN
	AR5B125	RALINK RT5390
VENDOR ID :	0X168C	0X1814
DEVICE ID :	0X0032	0X539A
(SSID) SUBSYSTEM ID :	0X1838	0X1839
SUBSYSTEM VENDOR ID :	0X103C	0X103C
HP P/N :	670036-001	670285-001

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
WLAN & BT

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	A01

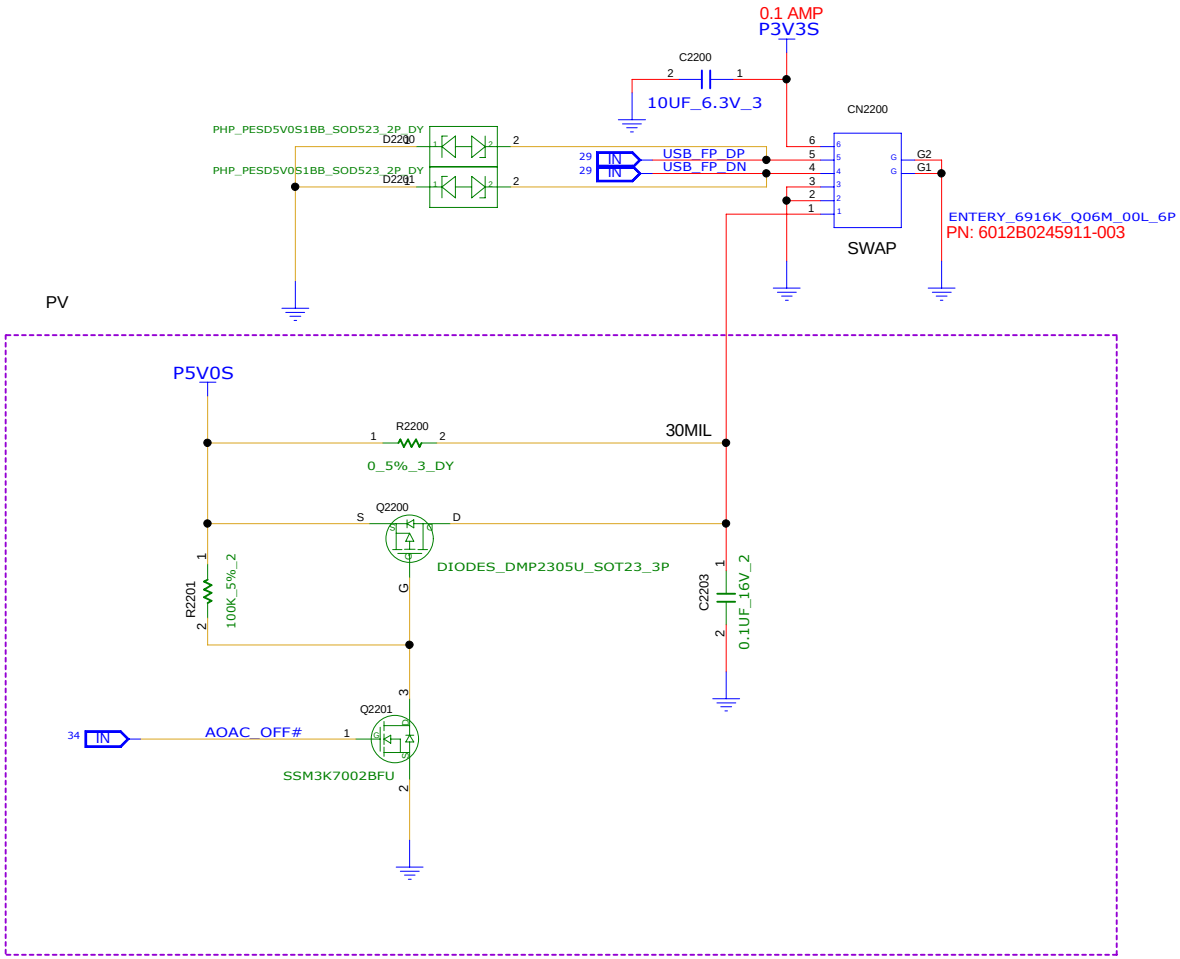
CHANGE by XXX | DATE 21-OCT-2002 | SHEET 44 of 70

FINGER PRINT

VFM5302-3192 PIN ASSIGNMENTS

Pin Number	Signal Name	Test Point
1	3.3V_{CC}	TP3
2	DP	TP1
3	DM	TP2
4	GND	TP4
5	GND	TP4
6	5V_{CC}	TP6

Figure 4 - Connector Pin-out

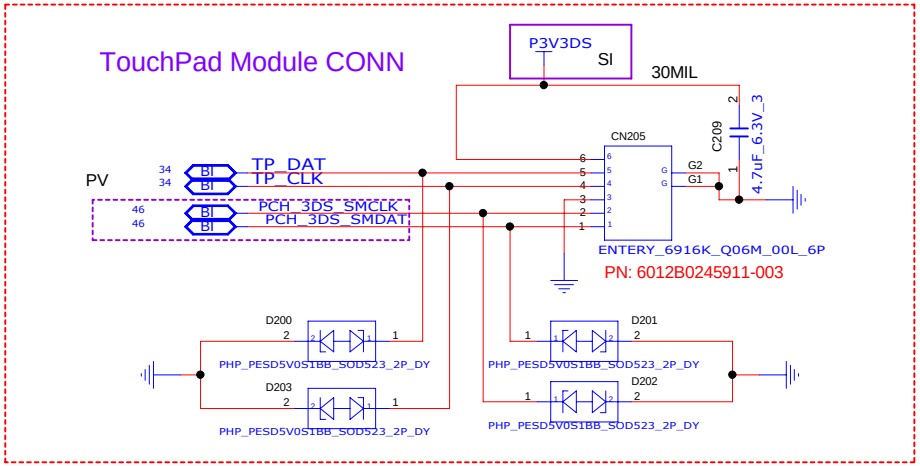


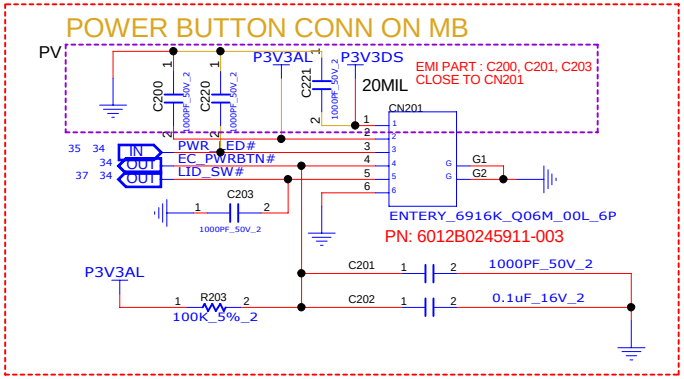
INVENTEC

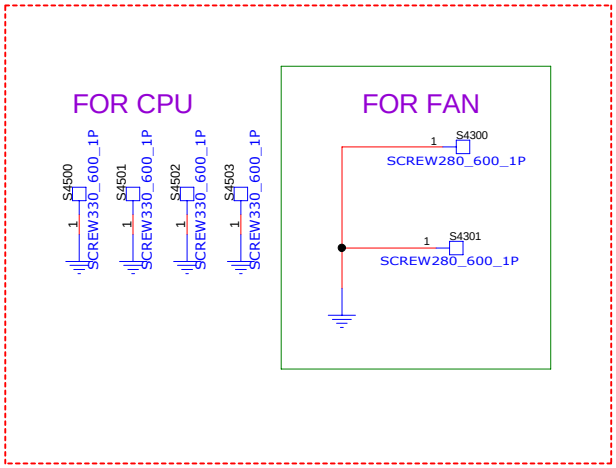
TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

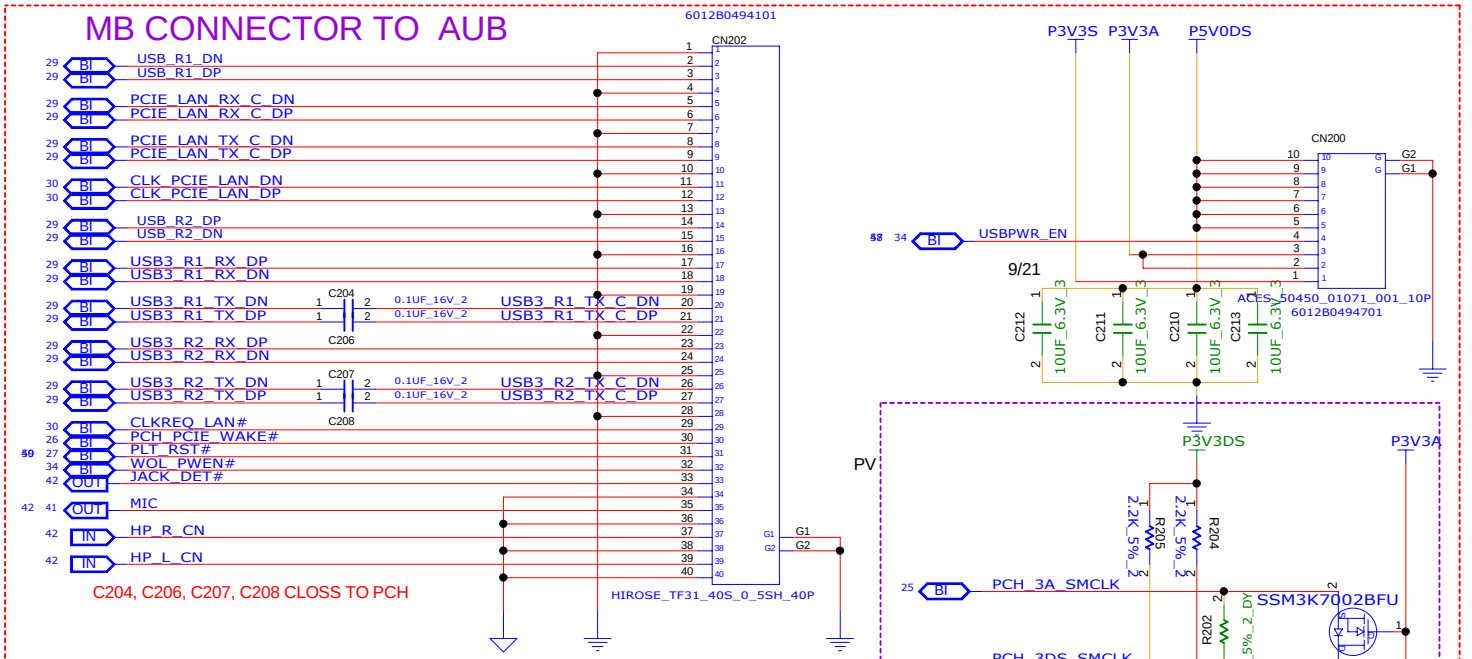
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	A01

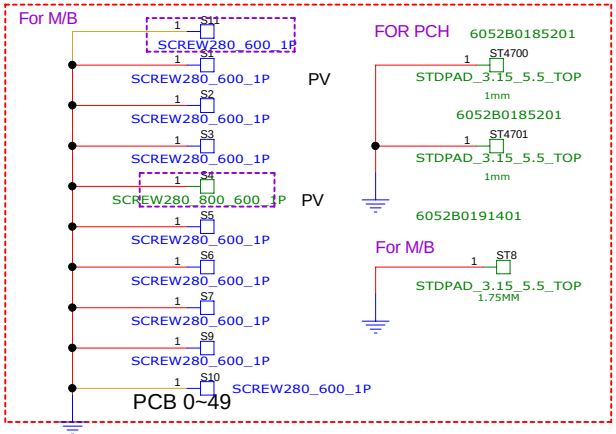
CHANGE by xxx | DATE 21-OCT-2002 | SHEET 45 of 70

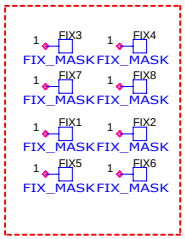












INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
POWER_BUTTON

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	A01

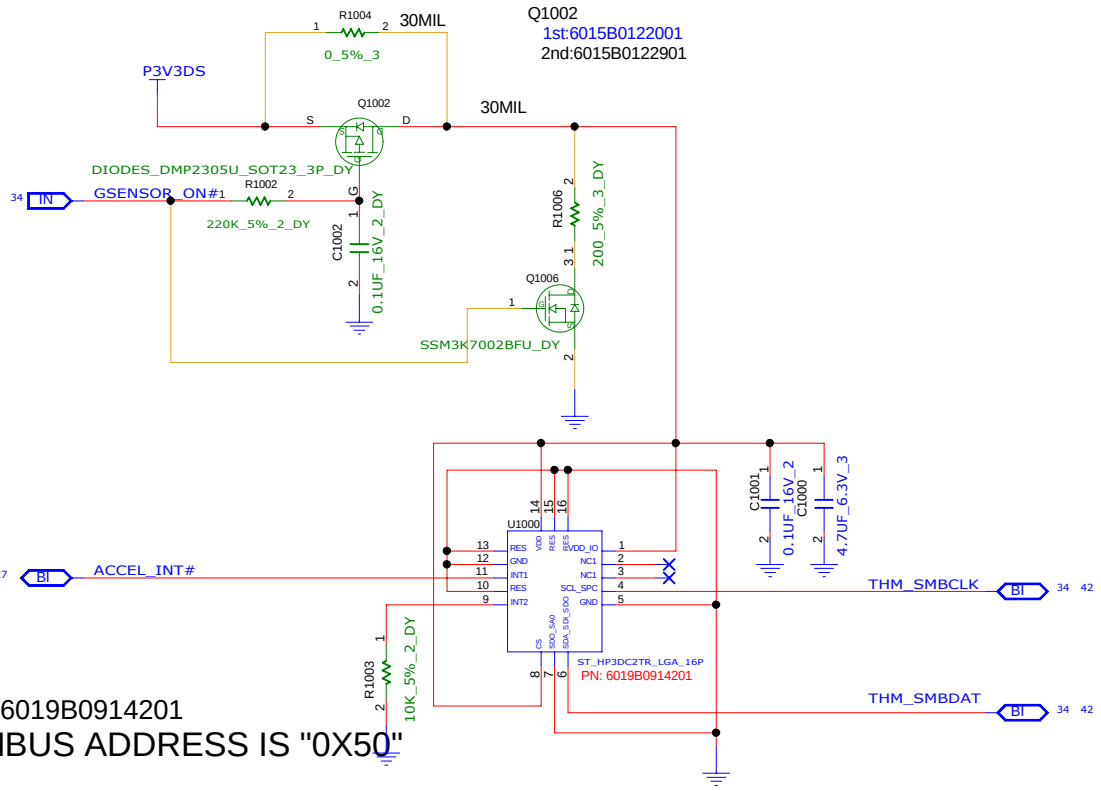
CHANGE by XXX | DATE 21-OCT-2002 | SHEET 46 of 70

G-Sensor

Loctaion 1000 ~ 1099

Ver.01_20120807

HARDDRIVE PROTECTION



PN:6019B0914201

SMBUS ADDRESS IS "0X50"

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	A01

CHANGE by XXX DATE 21-OCT-2002 SHEET 47 of 70

1ST: 6019B1012901 BCD AP2820AMMTR-
2ND: 6019B0947301 ROHM BD82024FVJ-E
3TH: 6019B0975501 NCT NCT3520W-H15

2.5 AMP

Location	Part number	Factory	Manufacturer Part No	Color
D9400	6011B0115101	EVERLIGHT	T3D_CP1Q2B12Y_2C	White
D9401	6011B0101001	EVERLIGHT	S2C_AL1M2VY_3C	Amber

USB 3.0 CONN

USB CHARGING TPS2546

PN: 6019B1035901

S0: 1
S3, S5: 0

SIZE IS 0805

CHANGE by	XXX
DATE	21-OCT-2002

INVENTEC

TITLE: MODEL PROJECT FUNCTION
USB 3.0 CONN & M/B TO D/B CONN

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	A01

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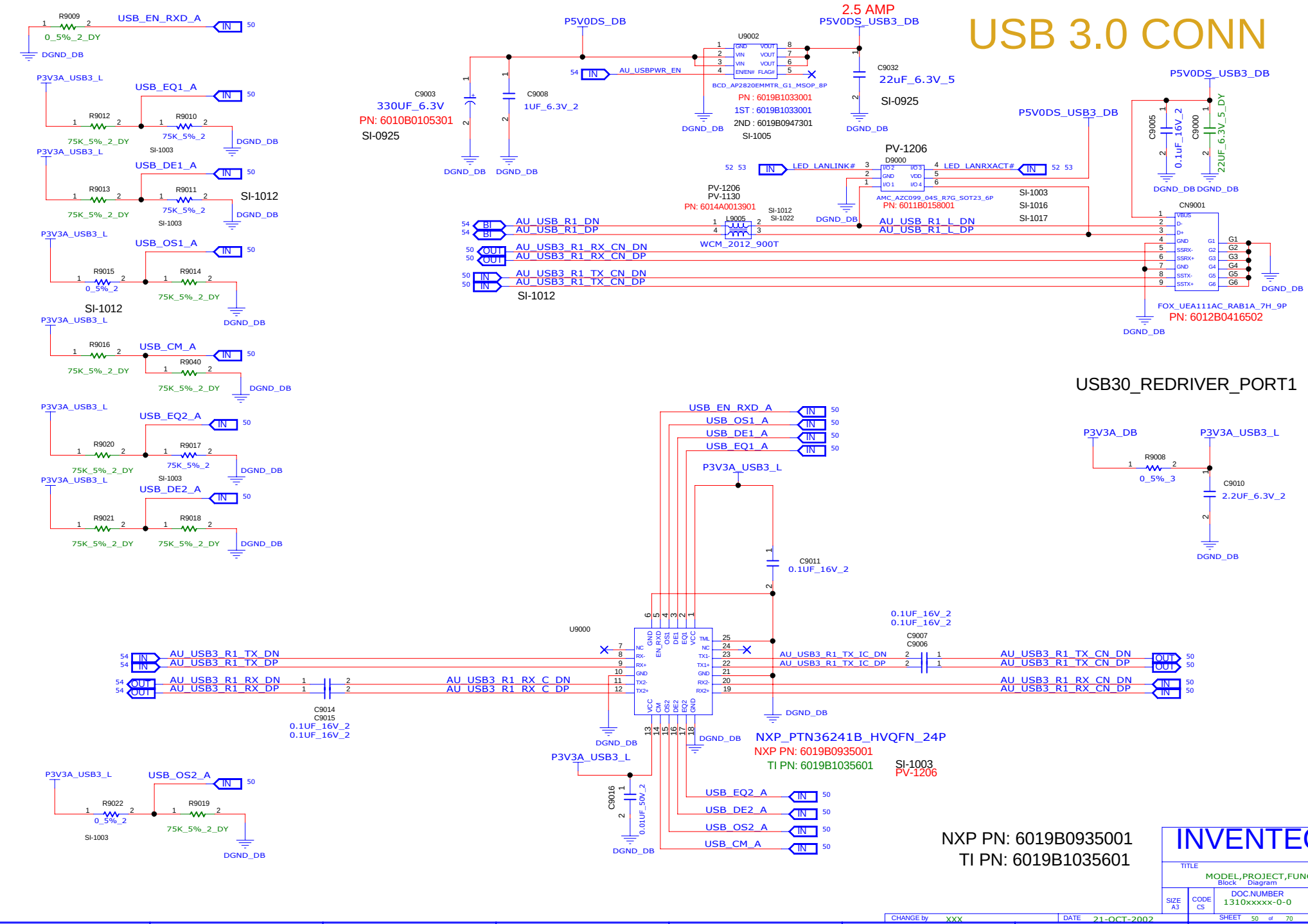
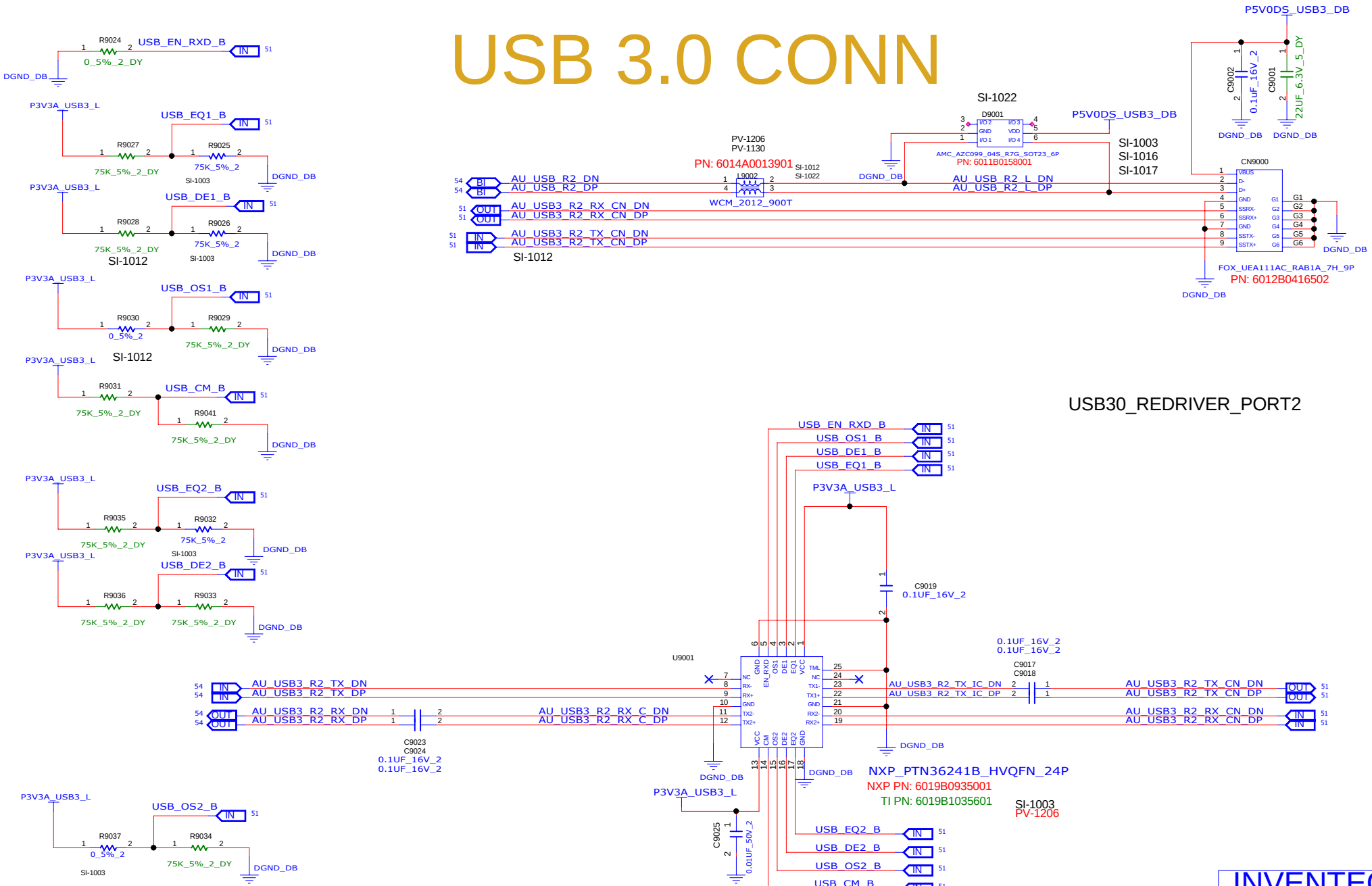
AUB BOARD

INVENTEC	
TITLE	MODEL,PROJECT,FUNCTION Block Diagram
SIZE A3	CODE CS
DOC.NUMBER	1310xxxxx-0-0
REV	A01
CHANGE by	XXX
DATE	21-OCT-2002
SHEET	49 of 70

USB 3.0 CONN



USB 3.0 CONN



ELMO (CR/SB UMA) 6L 1310A2548501 6050A2548501

ELMO (CR/SB DIS) 8L 1310A2548601 6050A2548601

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

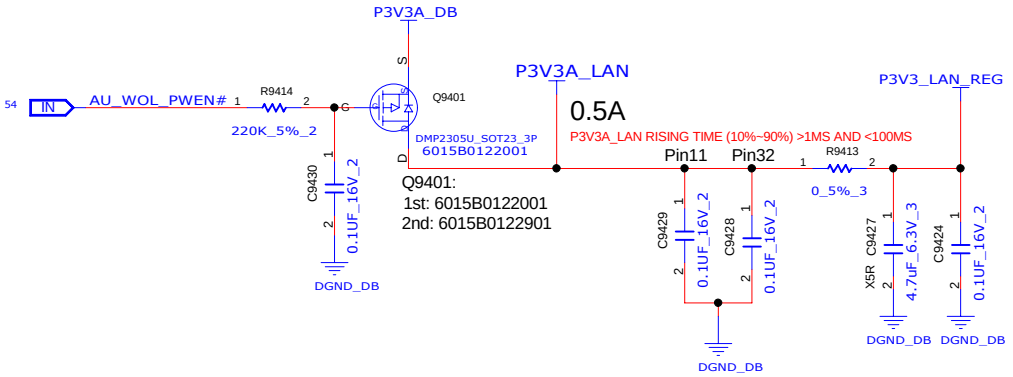
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	A01

CHANGE by: XXX DATE: 21-OCT-2002 SHEET 51 of 70

LAN (Controller)

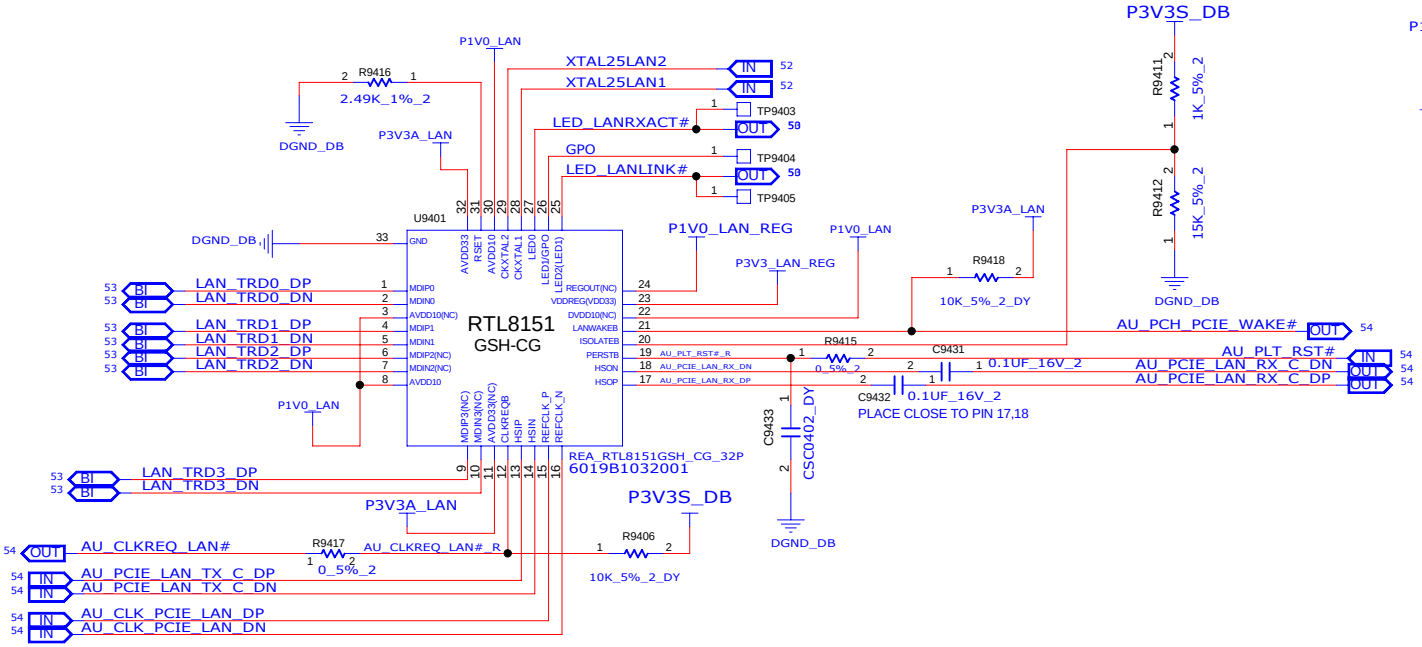
Location 9400 ~ 9499

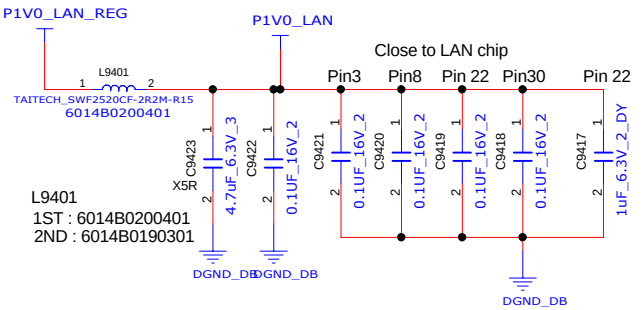
Ver.03_20120807

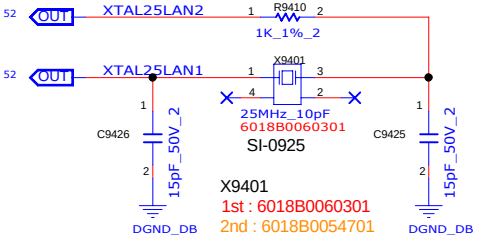


6019B1032101_RTL8161GSH-CG_10/100/1000

6019B1032001_RTL8151GSH-CG_10/100/1000







INVENTEC

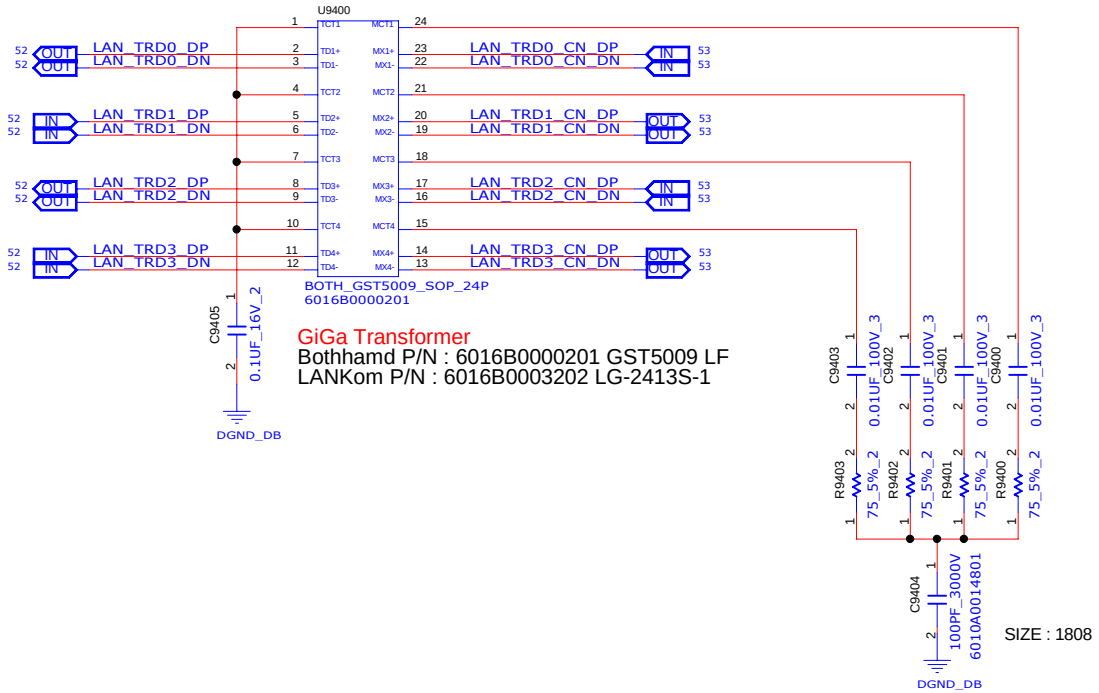
TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	A01

CHANGE by XXX | DATE 21-OCT-2002 | SHEET 52 of 70

LAN (Transformer & RJ45)

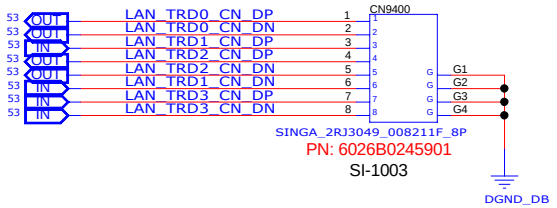
Location 9400 ~ 9499
Ver.06_20120813



GiGa Transformer
Bothhamd P/N : 6016B0000201 GST5009 LF
LANKom P/N : 6016B0003202 LG-2413S-1

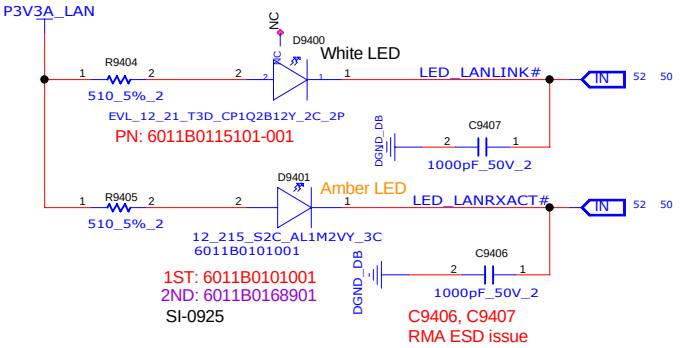
SIZE : 1808

RJ-45



PN: 6026B0245901
SI-1003

★Layout
D9400 White LED place on TOP side.
D9401 Amber LED place on Bottom side.



PN: 6011B0115101-001

1ST: 6011B0101001
2ND: 6011B0168901
SI-0925

C9406, C9407
RMA ESD issue

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	A01

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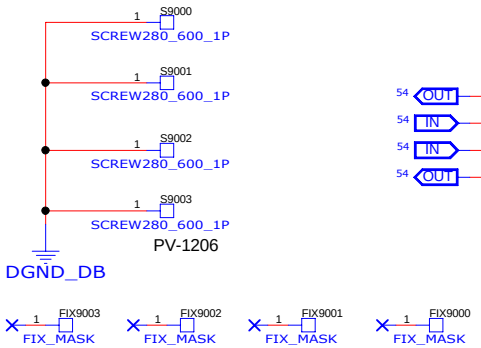
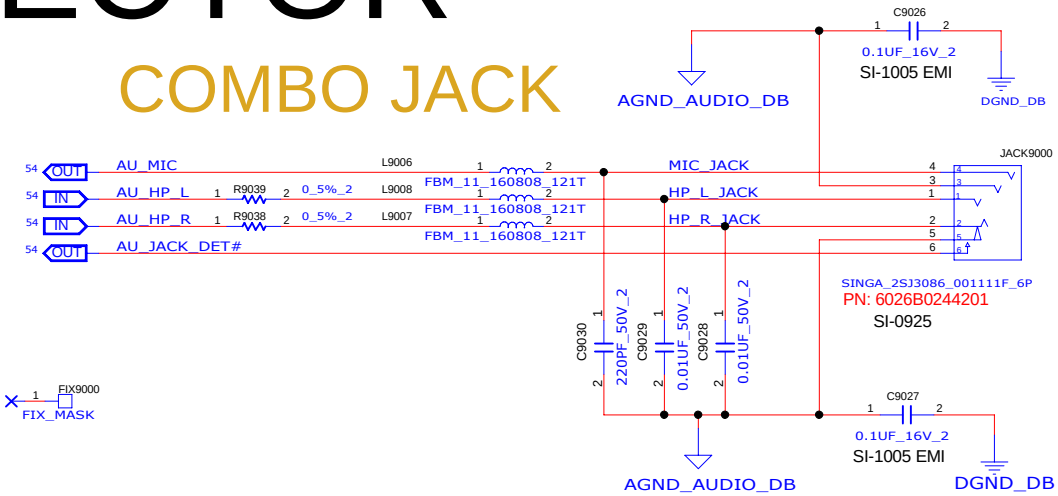
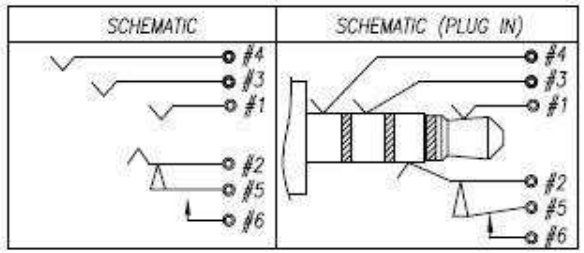
CONNECTOR

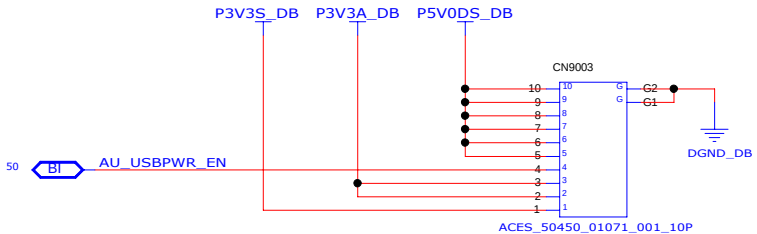
COMBO JACK

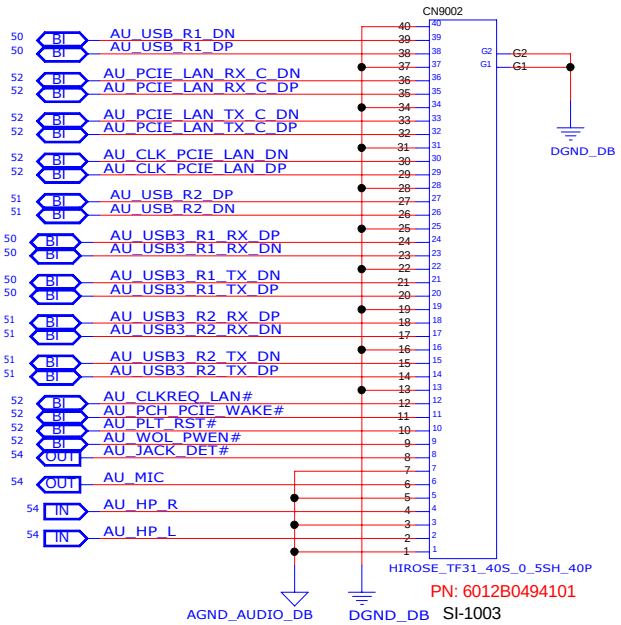






MB TO AUB CONNECTOR





INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	A01

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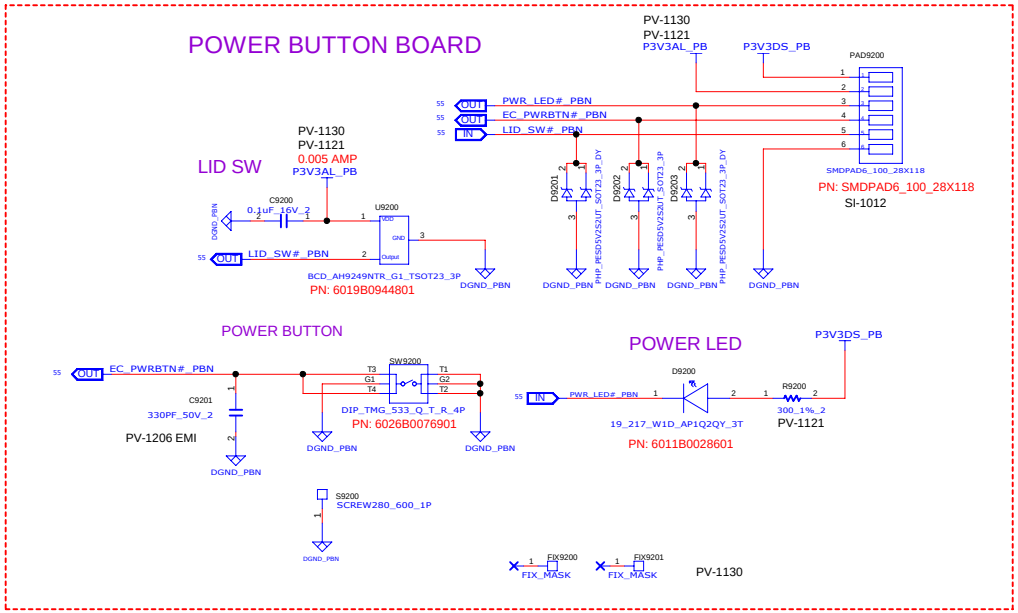
POWER BUTTON BOARD



INVENTEC

MODEL,PROJECT,FUNCTION

Block Diagram

SIZE	CODE	DOC.NUMBER	REV
C	CS	1310xxxxx-0-0	A01

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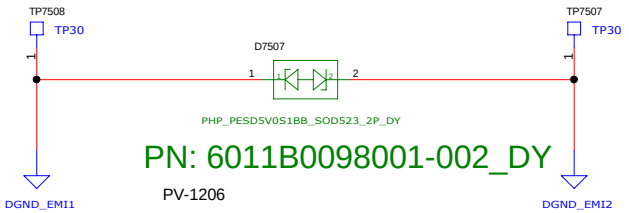
1310A2552101 (6L)
1310A2552201 (8L)

ESD BOARD 1

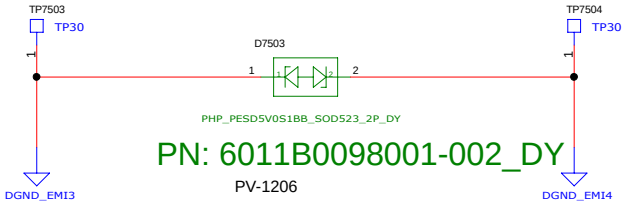


PN: 6011B0098001-002_DY

PV-1206

1310A2552102 (6L)
1310A2552202 (8L)

ESD BOARD 2



PN: 6011B0098001-002_DY

PV-1206

USB BOARD (6L)	1310A2548501	6050A2548501
USB BOARD (8L)	1310A2548601	6050A2548601
POWER BOARD (6L)	1310A2548701	6050A2548701
POWER BOARD (8L)	1310A2548801	6050A2548801
EMI BOARD (6L)	1310A2552101 1310A2552102	6050A2552101
EMI BOARD (8L)	1310A2552201 1310A2552202	6050A2552201

CHIEF RIVER	DIS	NVIDIA N14P-GV2 (GEFORCE 630M)	4G	SAMSUNG K4W4G1646B-HC11	1310A2548301
CHIEF RIVER	DIS	NVIDIA N14P-GV2 (GEFORCE 630M)	2G	MICRON MT41K256M16HA-107G:E	1310A2548302
CHIEF RIVER	UMA	N/A	N/A	N/A	1310A2548201

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	A01

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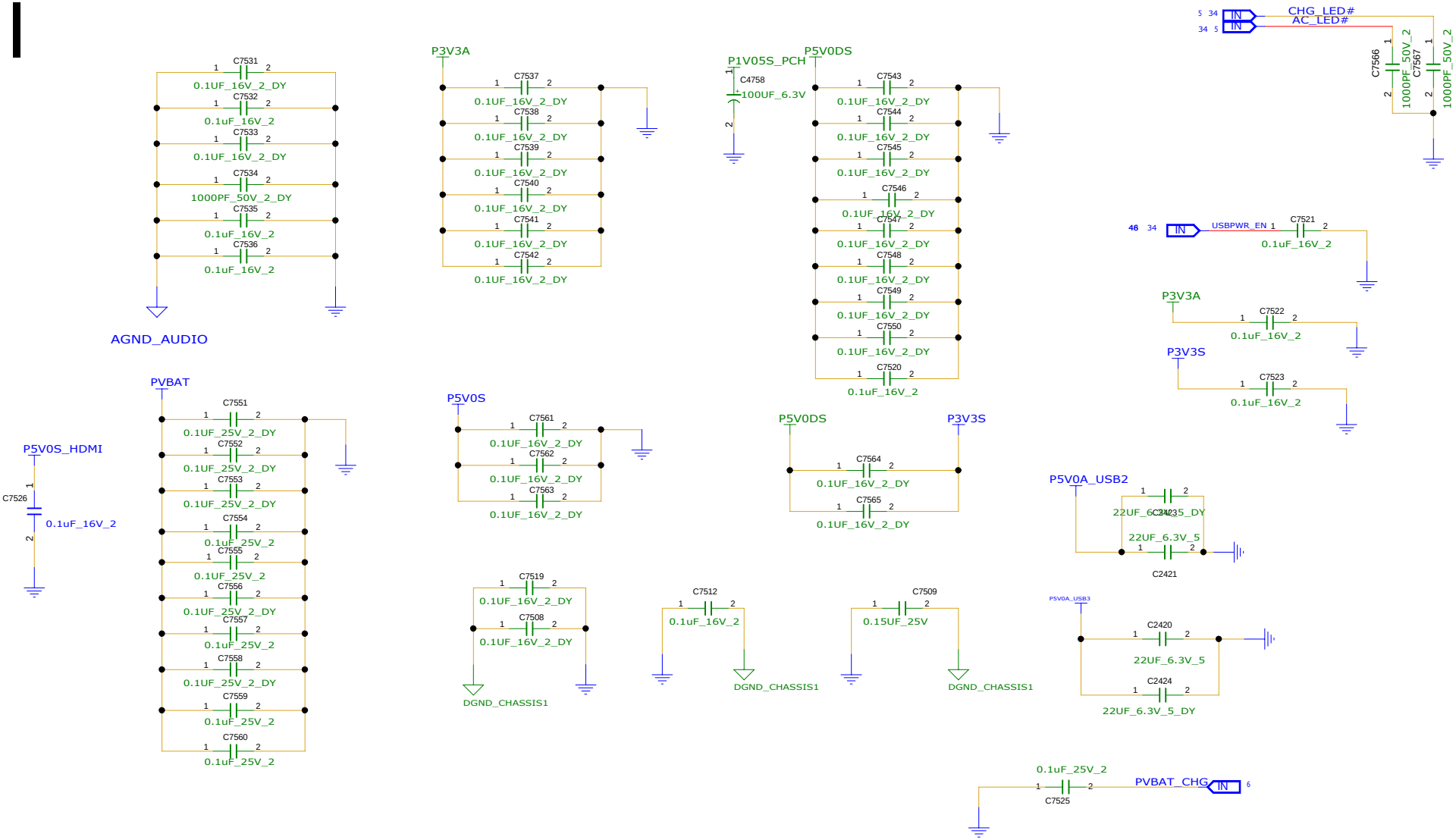
EMI



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	A01

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GPU

Location:GPU 5000~5499 VRAM 5500~5799 GPU SWITCH 7400~7499

VER.11_20120824

N14P-GV2 GB2-64 25W DUAL RANK DDR3

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	A01

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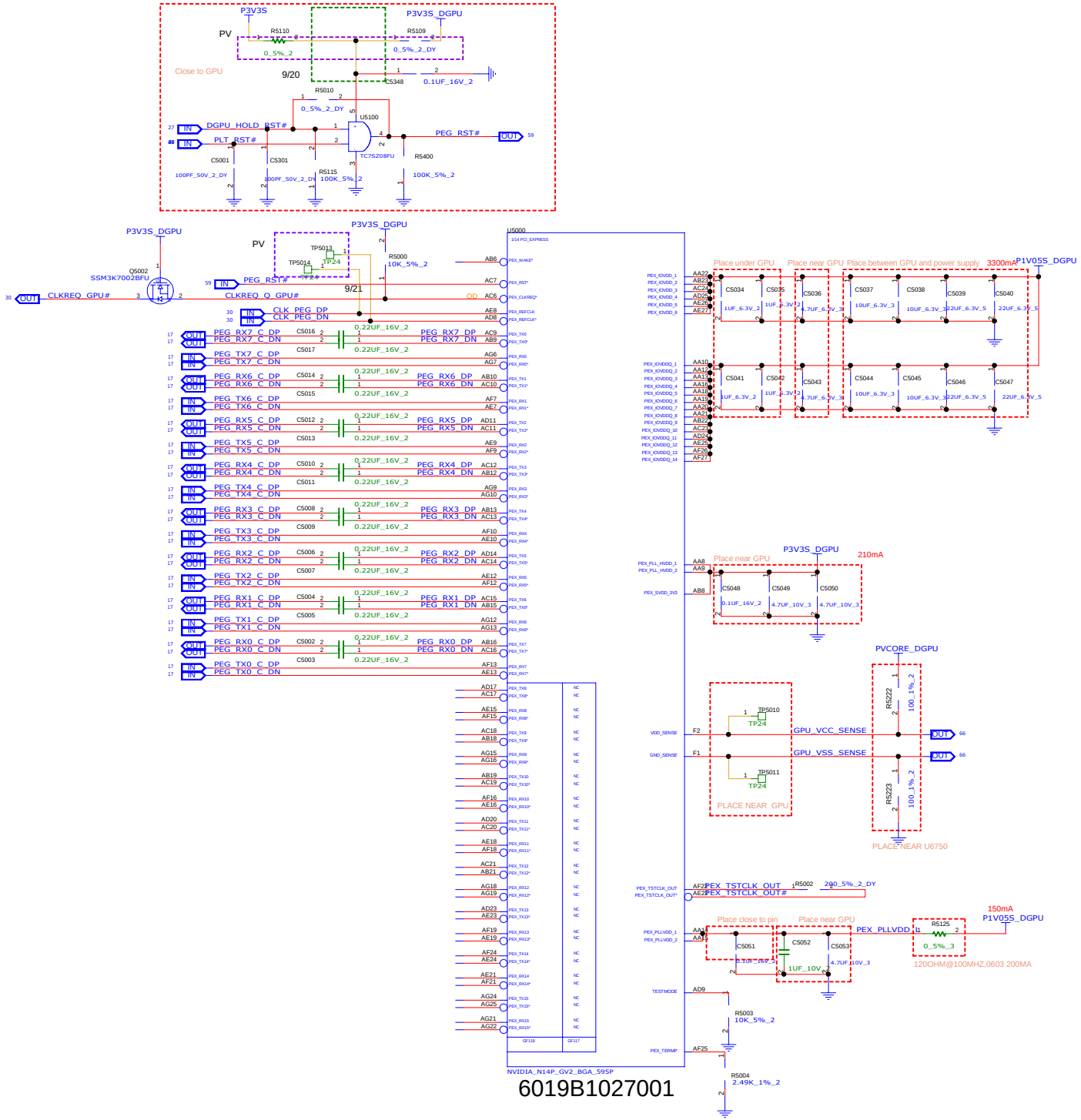

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
GPU-1

SIZE	CODE	DOC.NUMBER	REV
C	CS	1310xxxxx-D-D	A01

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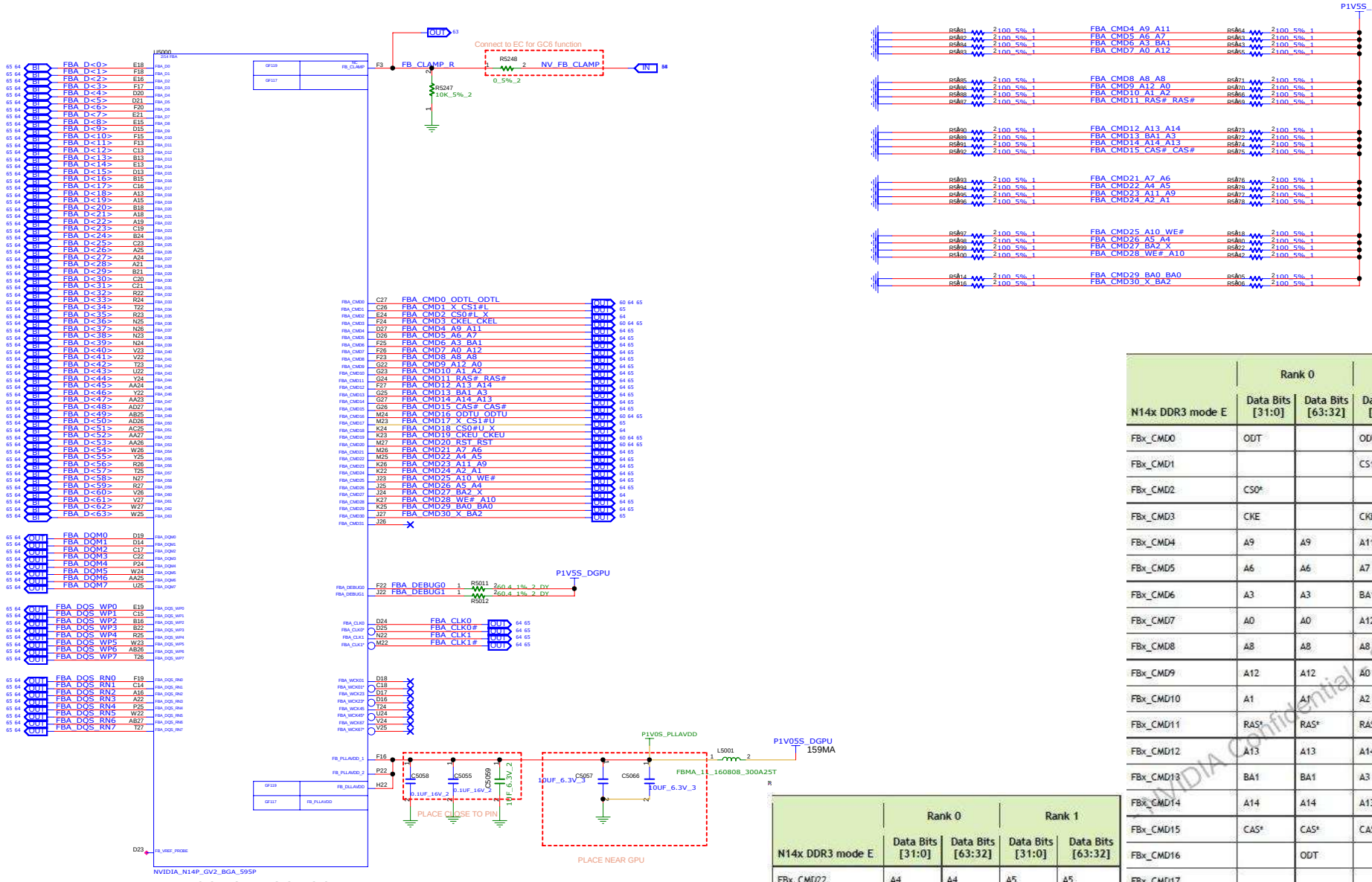
CHANGE by XXX DATE 21-OCT-2002



N14x DDR3 mode E	Rank 0		Rank 1	
	Data Bits [31:0]	Data Bits [63:32]	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	ODT		ODT	
FBx_CMD1			CS1*	
FBx_CMD2	CS0*			
FBx_CMD3	CKE		CKE	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS*	RAS*	RAS*	RAS*
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS*	CAS*	CAS*	CAS*
FBx_CMD16		ODT		ODT
FBx_CMD17				CS1*
FBx_CMD18		CS0*		
FBx_CMD19		CKE		CKE
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6

N14x DDR3 mode E	Rank 0		Rank 1	
	Data Bits [31:0]	Data Bits [63:32]	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE*	WE*
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE*	WE*	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2
FBx_CMD31				

INVENTEC

MODEL,PROJECT,FUNCTION
GPU-2

SIZE	CODE	DOC.NUMBER	REV
C	CS	1319xxxxx-0-0	A01

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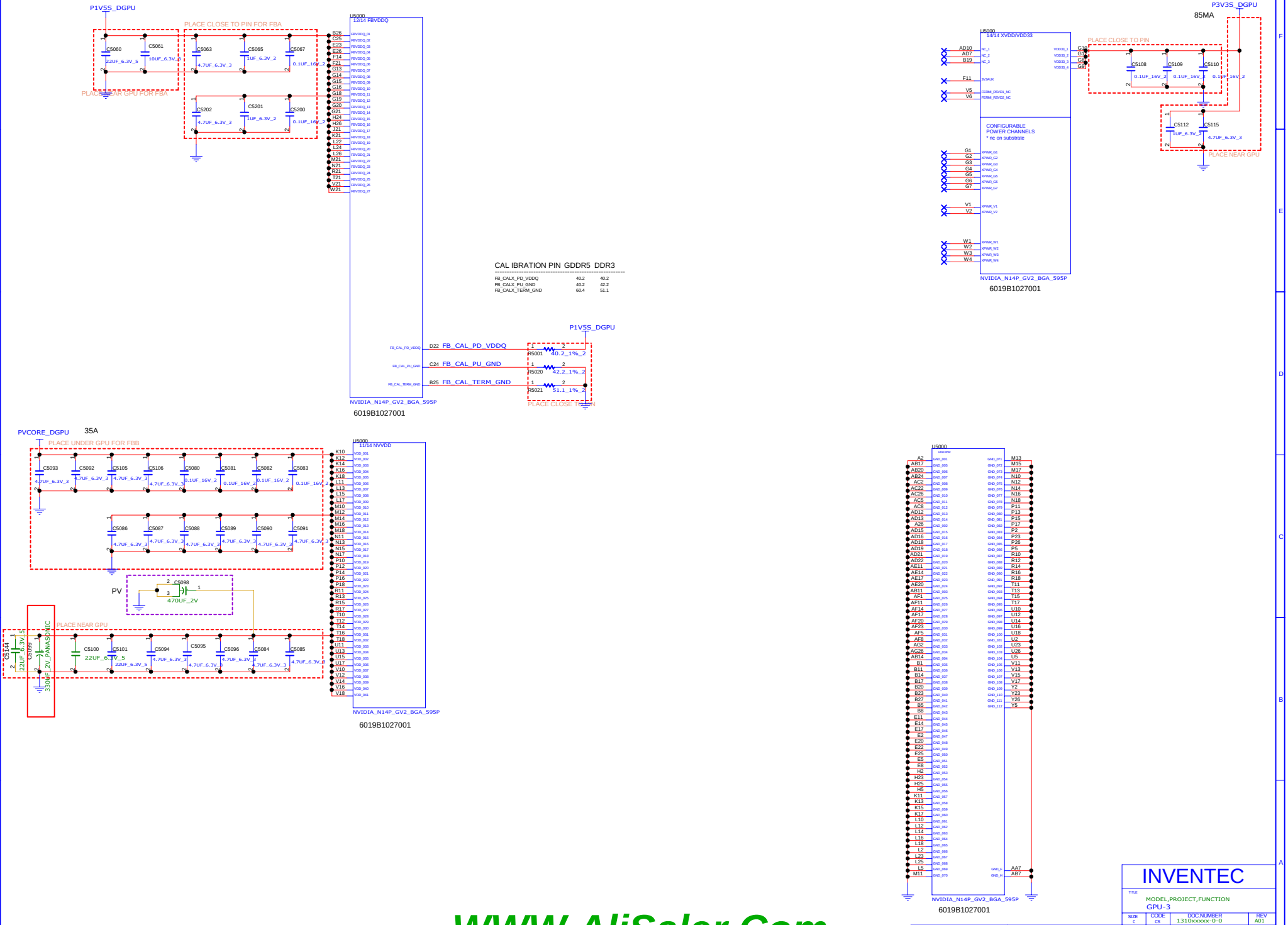
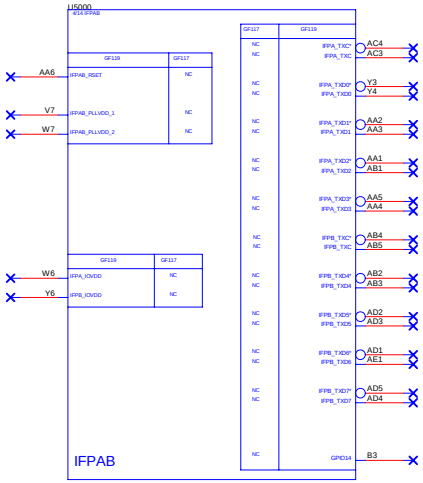
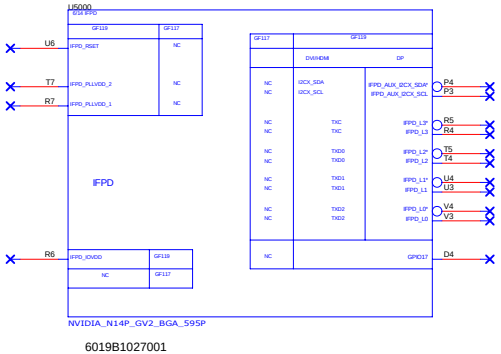
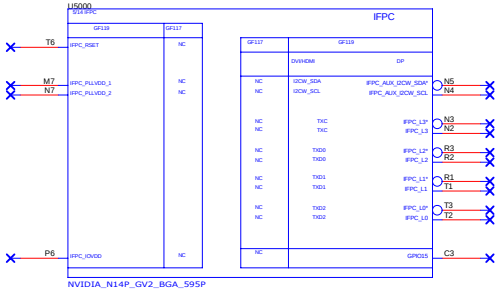
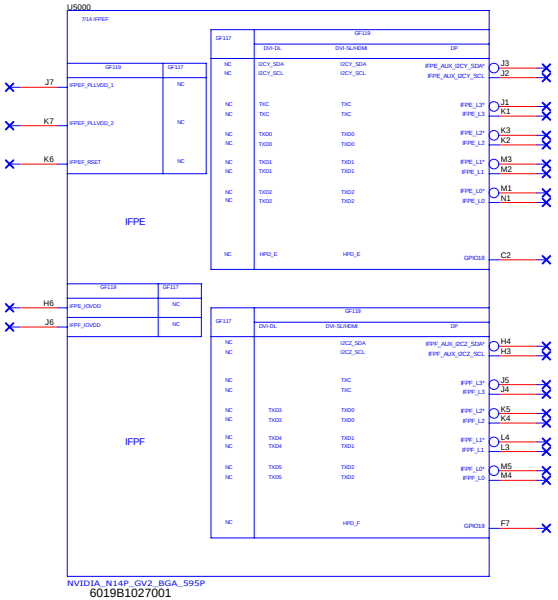
DATE 21-OCT-2012











INVENTEC

MODEL,PROJECT,FUNCTION
GPU-4

SIZE	CODE	DOC.NUMBER	REV
C	CS	1310xxxxx-0-0	A01

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Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

STRAP1	Description
0110	Gen 1/ Gen 2 support only
0000	Gen 3 support
Other settings	RESERVED

STRAP3		HDMI/DP	DVI	LVDS	eDP	Not In Use
Standard Mode	IFPA/B			SOR0_EXP = 0		SOR0_EXP = 0
	IFPC	SOR1_EXP = 1				SOR1_EXP = 0
	IFPD	SOR1_EXP = 1			SOR2_EXP = 0	SOR2_EXP = 0
	IFPE/F	SOR3_EXP = 1	SOR3_EXP = 1			SOR3_EXP = 0
Split Mode	IFPA/B					
	IFPC	SOR1_EXP = 1				SOR1_EXP = 0
	IFPD	SOR1_EXP = 1			SOR2_EXP = 0	SOR2_EXP = 0
	IFPE	SOR3_EXP = 1				SOR3_EXP = 0
	IFPF	SOR0_EXP = 1				SOR0_EXP = 0
Combined Mode	IFPA	SOR3_EXP = 1	SOR0_EXP = 1	SOR0_EXP = 0		SOR0_EXP = 0
	IFPB	SOR0_EXP = 1				SOR1_EXP = 0
	IFPC	SOR1_EXP = 1				SOR2_EXP = 0
	IFPD	SOR2_EXP = 1			SOR2_EXP = 0	SOR3_EXP = 0

STRAP4	Configuration
0000 5K	reserved
0001 10K	reserve for PCIE GEN3 speed function 0 : default
0010 15K	
0011 20K	0 : limit to PCIE Gen1 1 : PCIE Gen2/3 capable
0100 25K	
0101 30K	reserve for future use 0 : default
0110 35K	
0111 45K	

RAMCFG[3:] ROM_SI	Configuration
0000 5K	<reserved>
0001 10K	<reserved>
0010 15K	<reserved>
0011 20K	<reserved>
0100 25K	<reserved>
0101 30K	Samsung 32Mx32
0110 35K	<reserved>
0111 45K	<reserved>

ROM_SO	Configuration
0000 5K	00, 01, 11 : reserved 10 : 256M frame buffer 0 : I2CS slave address=0x9E 1 : I2CS slave address=0x9C 0 : 3D device 1 : VGA device
0001 10K	
0010 15K	
0011 20K	
0100 25K	
0101 30K	
0110 35K	
0111 45K	

ROM_SCLK	Configuration
0000 5K	GPU device ID 0 : No VBIOS ROM 1 : VBIOS ROM is present 0 : Disable PCIE PLL termination 1 : Enable PCIE PLL termination
0001 10K	
0010 15K	
0011 20K	
0100 25K	
0101 30K	
0110 35K	
0111 45K	

VENDER	DENSITY	VENDER PN	IEC PN	STRAP	R5061
SAMSUNG	128MX16	K4W2G1646E-BC1A	6019B1033601	0X7	45.3K
MICRON	128MX16	MT41K128M16JT-093G:K	6019B1033501	0X5	30.1K

INVENTEC

MODEL,PROJECT,FUNCTION
GPU-5

SIZE C | CODE CS | DOC NUMBER 1310xxxxx-0-0 | REV A01

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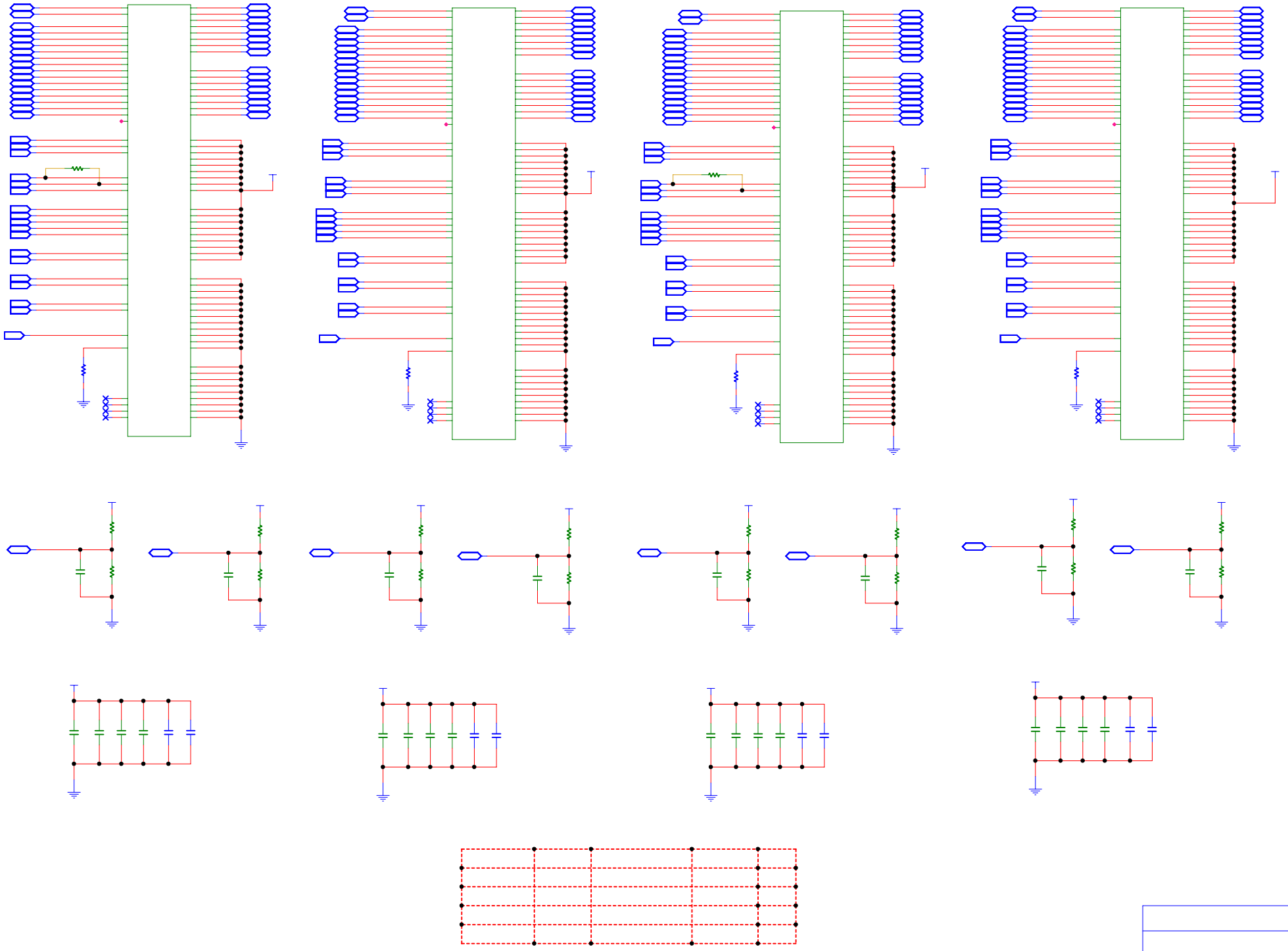
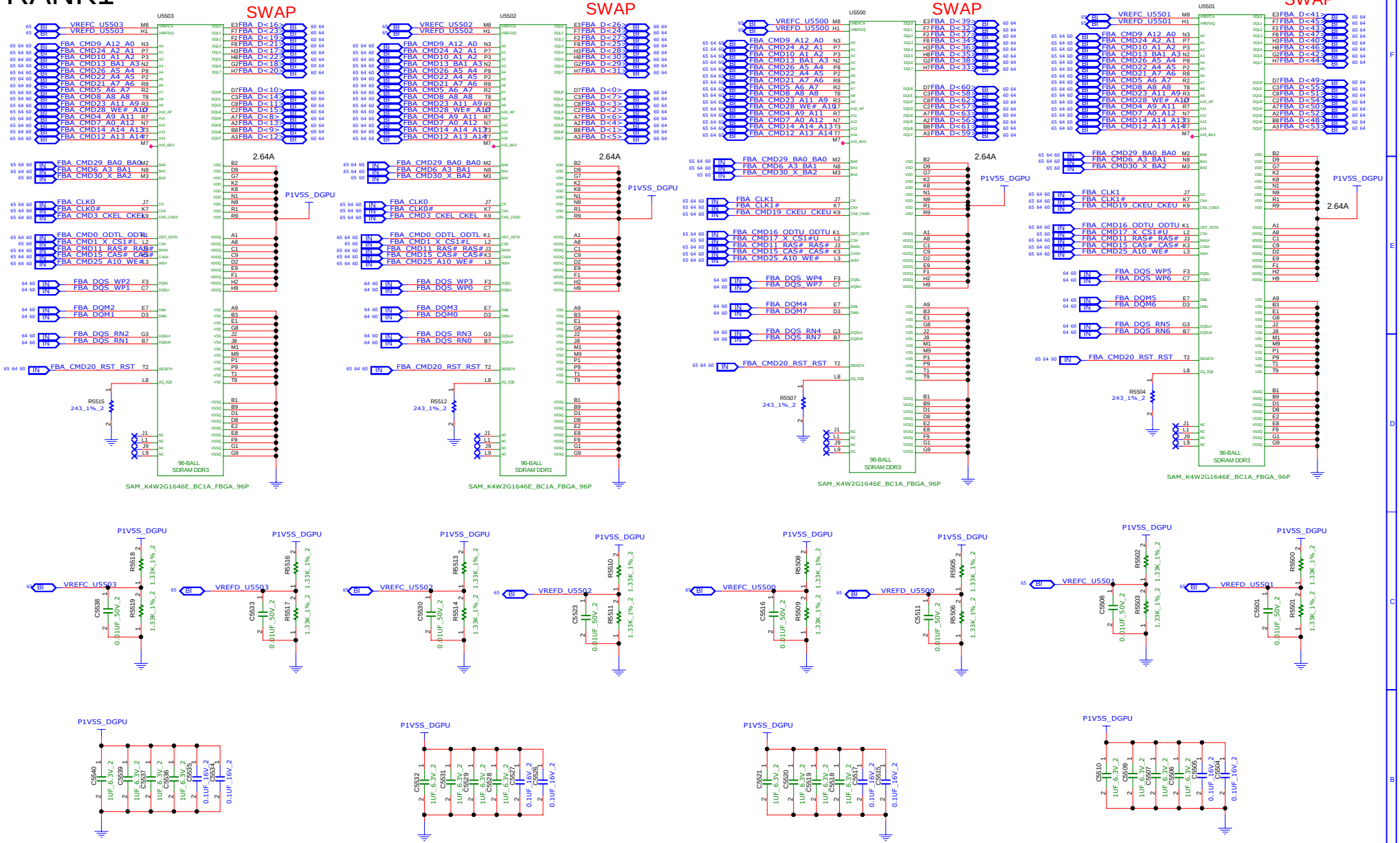


RANK1



CHANNEL A MEMORY

VENDER	DENSITY	VENDER PN	IEC PN	STRAP
SAMSUNG	128MX16	K4W2G1646E-BC1A	6019B1033601	0X7
MICRON	128MX16	MT41K128M16JT-093G:K	6019B1033501	0X5

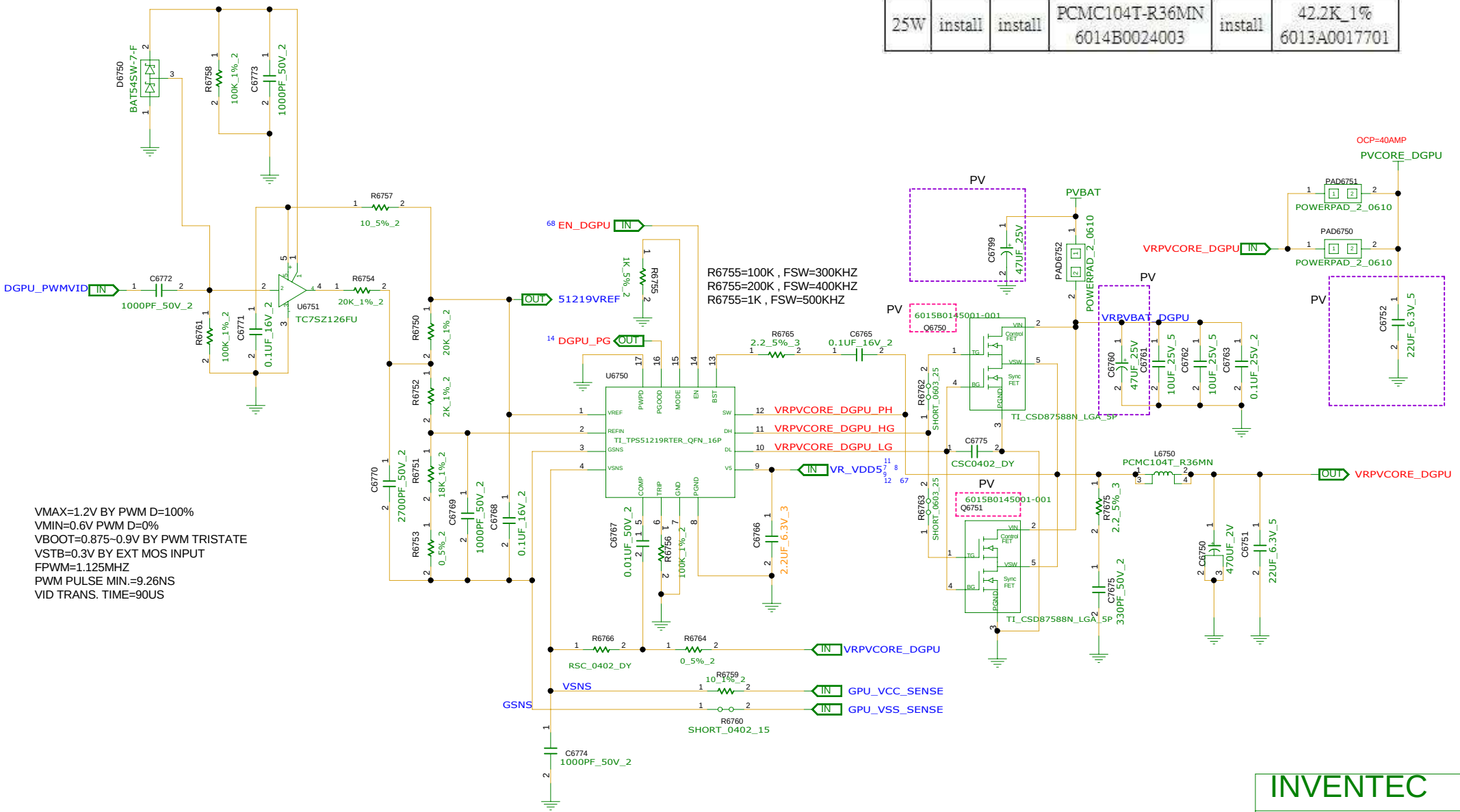
INVENTEC

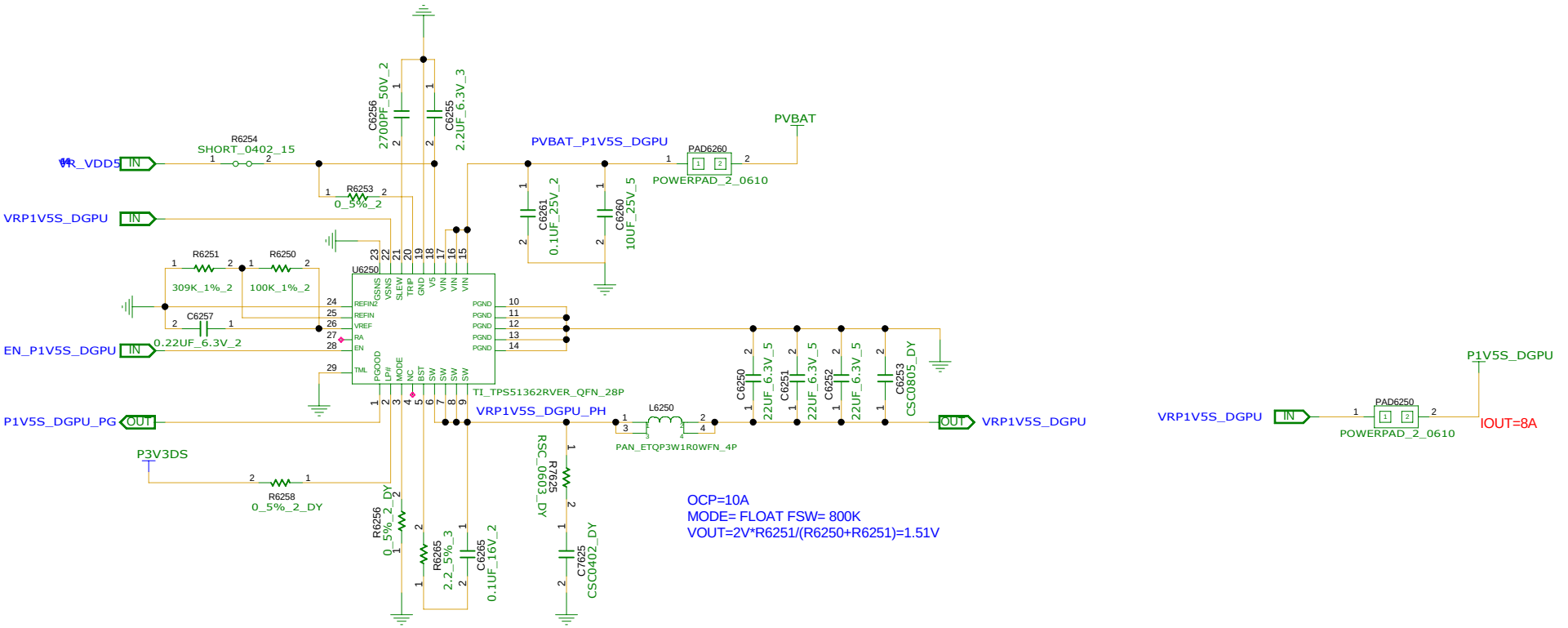
TITLE: MODEL,PROJECT,FUNCTION
VRAM DDR3

SIZE: C | CODE: CS | DOC NUMBER: 1310xxxxx-0-0 | REV: A01

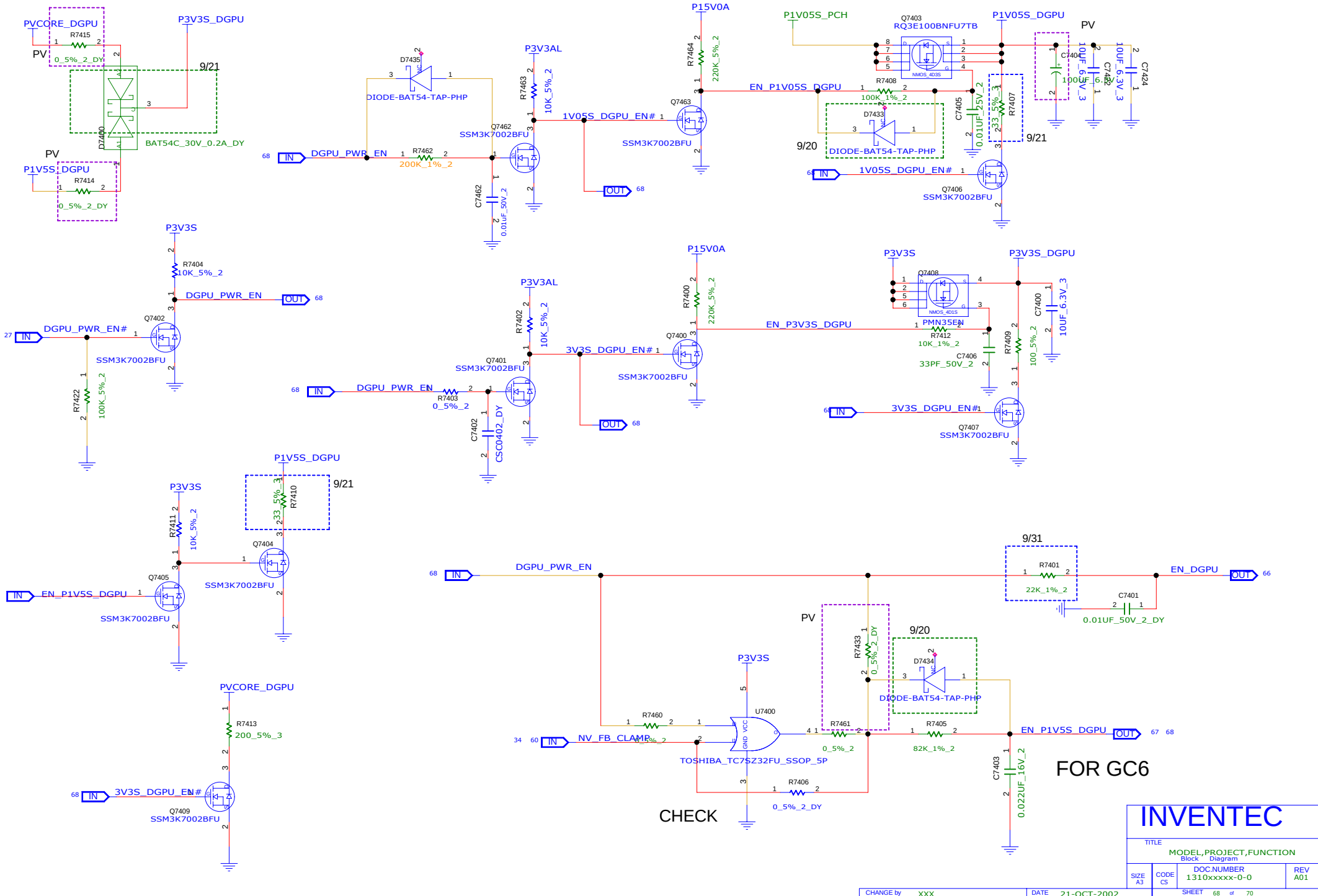
CHANGE by: YXX | DATE: 21-OCT-2002 | SHEET 65 of 79

	C6762	C6752	L6750	Q6751	R6756
17W	OPEN	OPEN	ETQP4LR36AFM 6014B0164501	OPEN	80.6K_1% 6013A0072901
25W	install	install	PCMC104T-R36MN 6014B0024003	install	42.2K_1% 6013A0017701





INVENTEC			
TITLE MODEL,PROJECT,FUNCTION SYSTEM POWER(P1V05_LAN_M)			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV A01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 67 of 70	



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	A01

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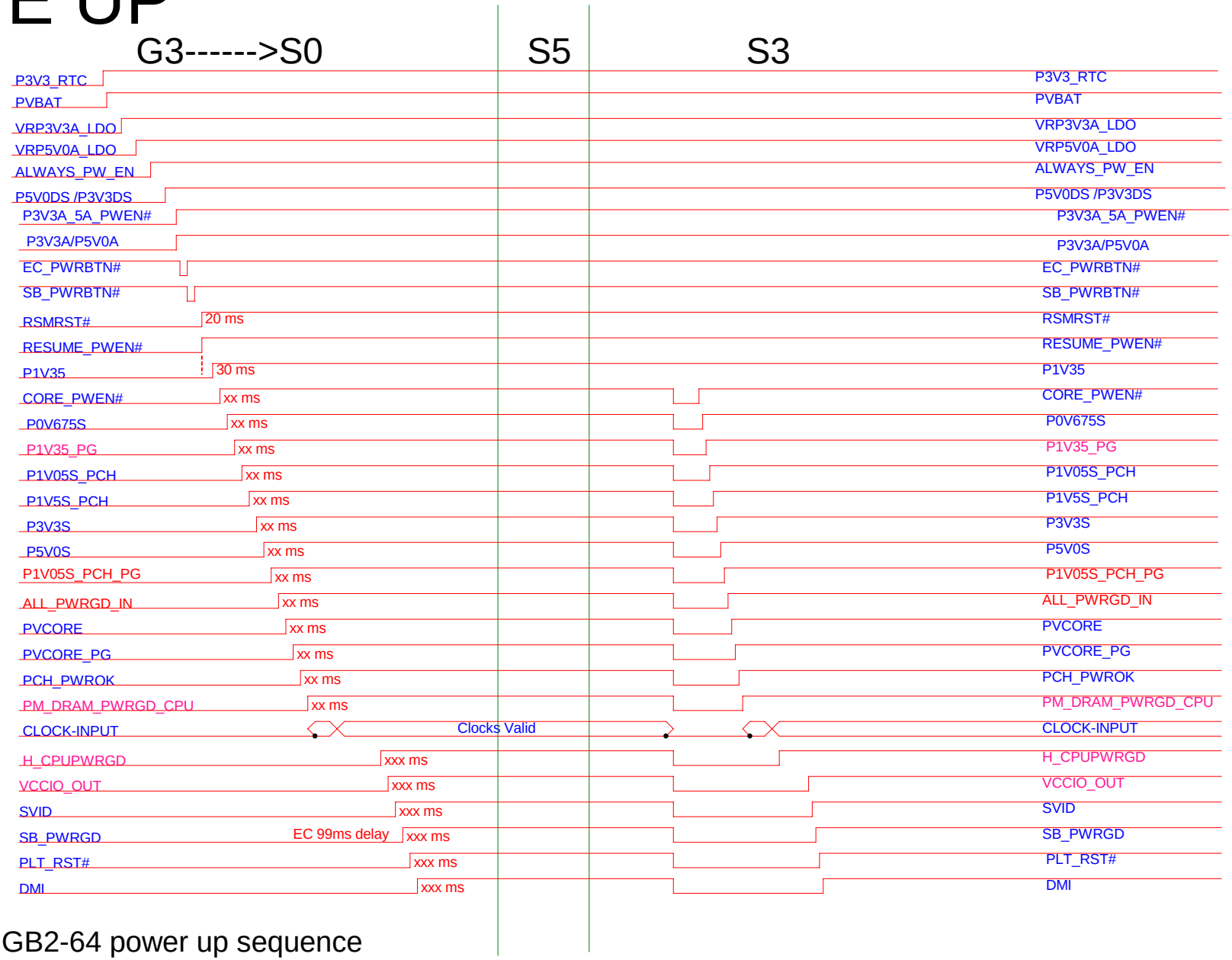
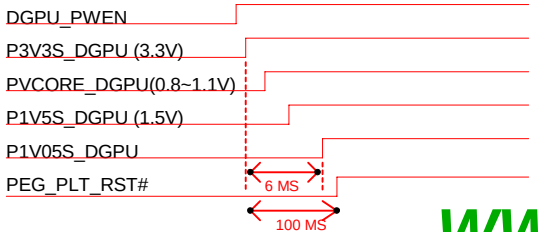
POWE UP



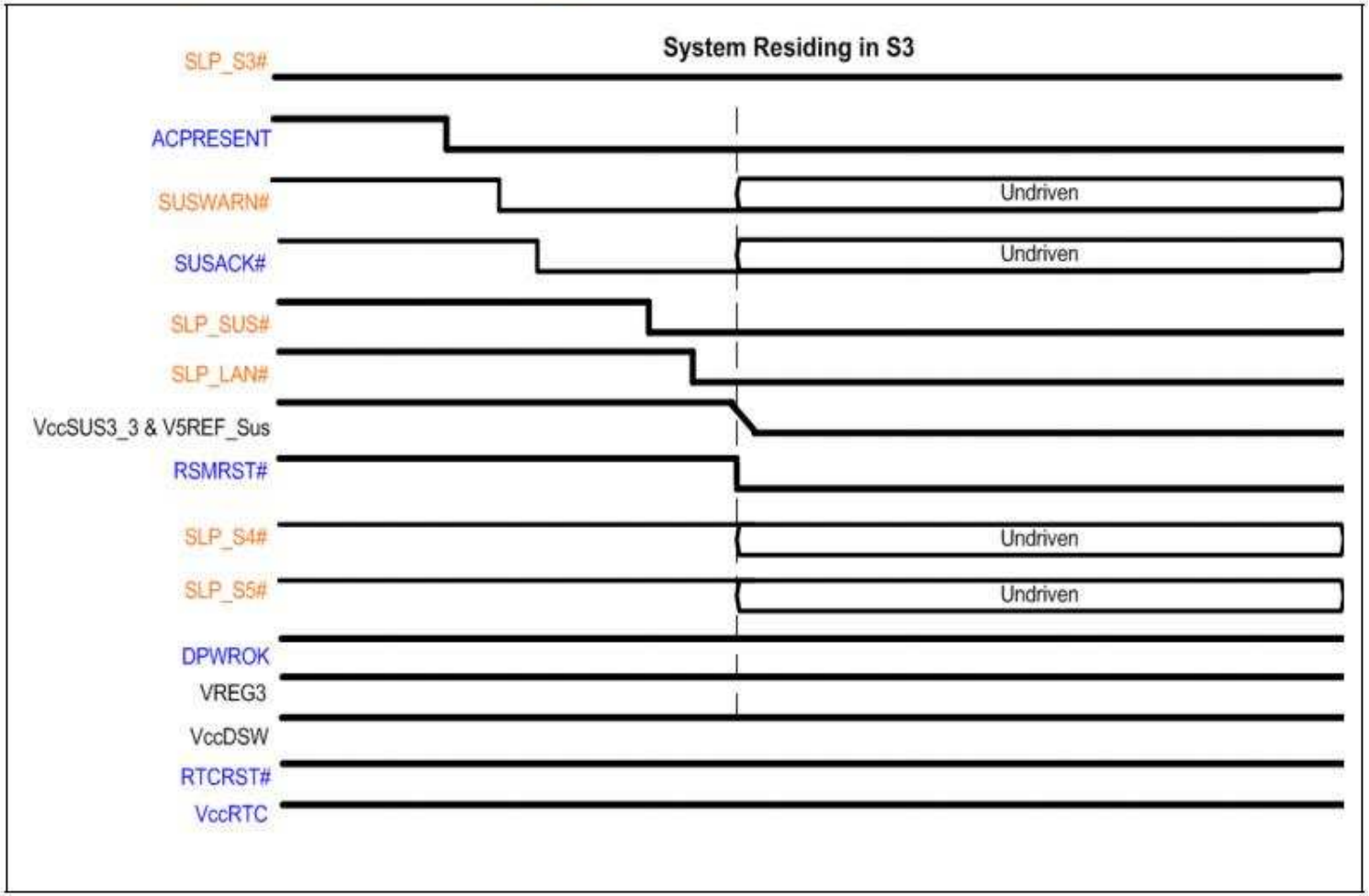
NV N14P GB2-64 power up sequence



INVENTEC

MODEL,PROJECT,FUNCTION
Block Diagram

S3 to Deep S3 Transition on AC_PRESENT Low



INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	A01

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